

	L #	Hits	Search Text	DBs
1	L1	12017	(queue buffer fifo) near5 instruction	USPAT; US-PGPUB
2	L3	14667	(issu\$3 dispatch\$3 schedul\$3 execut\$3) near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent\$3 simultaneous\$3))	USPAT; US-PGPUB
3	L6	4226	(queue buffer fifo) near5 instruction	EPO; JPO; DERWENT; IBM_TDB
4	L7	3840	(issu\$3 dispatch\$3 schedul\$3 execut\$3) near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent\$3 simultaneous\$3))	EPO; JPO; DERWENT; IBM_TDB
5	L9	171	6 near99 7	EPO; JPO; DERWENT; IBM_TDB
6	L5	726	1 near99 3	USPAT; US-PGPUB

	Docum ent ID	U	Title	Current OR
1	JP 20031 14798 A	<input type="checkbox"/>	DATA PROCESSING METHOD FOR SUPERSCALAR PROCESSING SYSTEM	
2	JP 20030 67184 A	<input checked="" type="checkbox"/>	CHECKPOINTING OF SUPERSCALAR OUT-OF-ORDER PROCESSOR FOR ERROR RECOVERY	
3	JP 20023 18687 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR AND COMPUTER SYSTEM	
4	JP 20020 07118 A	<input checked="" type="checkbox"/>	VLIW PROCESSOR	
5	JP 20023 18687 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR AND COMPUTER SYSTEM	
6	JP 20020 07118 A	<input checked="" type="checkbox"/>	VLIW PROCESSOR	
7	JP 20012 43067 A	<input checked="" type="checkbox"/>	SUPER SCALAR PROCESSING SYSTEM AND DATA PROCESSING METHOD	
8	JP 20012 29023 A	<input checked="" type="checkbox"/>	SUPERSCALAR PROCESSING SYSTEM AND DATA PROCESSING METHOD	
9	JP 20012 16157 A	<input checked="" type="checkbox"/>	INSTRUCTION RETRIEVAL AND PORT ALLOCATION (FIAP) CIRCUIT AND ITS METHOD	
10	JP 20010 92657 A	<input checked="" type="checkbox"/>	CENTRAL ARITHMETIC UNIT AND COMPILE METHOD AND RECORDING MEDIUM RECORDING COMPILE PROGRAM	
11	JP 20003 39163 A	<input checked="" type="checkbox"/>	SUPER SCALAR MICROPROCESSOR, ITS PROCESSOR SYSTEM, DATA PROCESSING METHOD IN THE SAME AND COMPUTER SYSTEM PROVIDED WITH PROCESSOR	
12	JP 20003 39162 A	<input checked="" type="checkbox"/>	SUPER SCALAR MICRO PROCESSOR	
13	JP 20002 95289 A	<input checked="" type="checkbox"/>	LARGE COUPLING WIDE BAND OR NARROW BAND EXCHANGE	
14	JP 20002 76351 A	<input checked="" type="checkbox"/>	PROCESSOR HAVING LOCAL INSTRUCTION LOOPING	
15	JP 20001 48484 A	<input checked="" type="checkbox"/>	REGISTER NAME CHANGE SYSTEM	
16	JP 20000 39996 A	<input checked="" type="checkbox"/>	SUPERSCALAR PROCESSING SYSTEM AND DATA PROCESSING METHOD	
17	JP 20000 29698 A	<input checked="" type="checkbox"/>	SUPER SCALAR PROCESSING SYSTEM AND DATA PROCESSING METHOD	

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18	JP 20000 29697 A	<input checked="" type="checkbox"/>	SUPER SCALAR PROCESSOR, DATA PROCESSING METHOD AND COMPUTER SYSTEM	
19	JP 41134 5121 A	<input checked="" type="checkbox"/>	INSTRUCTION EXTRACTING DEVICE FOR PROGRAM CONTROL UNIT AND METHOD THEREOF	
20	JP 41131 6681 A	<input checked="" type="checkbox"/>	LOADING METHOD TO INSTRUCTION BUFFER AND DEVICE AND PROCESSOR THEREFOR	
21	JP 11289 348 A	<input checked="" type="checkbox"/>	PACKET EXCHANGE AND DATA TRANSMISSION PROCESSING METHOD THEREFOR	
22	JP 11259 644 A	<input checked="" type="checkbox"/>	IMAGE FORMING DEVICE AND IMAGE FORMING METHOD	
23	JP 11242 599 A	<input checked="" type="checkbox"/>	COMPUTER PROGRAM	
24	JP 11085 619 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
25	JP 11073 318 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
26	JP 10307 723 A	<input checked="" type="checkbox"/>	PROCESSOR	
27	JP 10207 708 A	<input checked="" type="checkbox"/>	PROGRAMMABLE CONTROLLER	
28	JP 10177 559 A	<input checked="" type="checkbox"/>	DEVICE, METHOD, AND SYSTEM FOR PROCESSING DATA	
29	JP 10091 436 A	<input checked="" type="checkbox"/>	PROGRAM LOADER	
30	JP 10003 425 A	<input checked="" type="checkbox"/>	INSTRUCTION SUPPLY DEVICE	
31	JP 09274 565 A	<input checked="" type="checkbox"/>	PIPELINED MICROPROCESSOR WITH NO INTERRUPTION CAUSED BY BRANCH AND OPERATING METHOD FOR THE SAME	
32	JP 09251 286 A	<input checked="" type="checkbox"/>	DISPLAY GRAPHIC ADAPTER IN WINDOW SYSTEM FOR PROCESSING DIFFERENT PIXEL SIZES AND METHOD FOR STORING PIXEL DATA	
33	JP 09114 660 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
34	JP 09022 354 A	<input checked="" type="checkbox"/>	METHOD AND DEVICE FOR EXECUTING INSTRUCTION SEQUENCE	
35	JP 09006 759 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	
36	JP 08314 720 A	<input checked="" type="checkbox"/>	BRANCH CONTROL SYSTEM	
37	JP 08249 228 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
38	JP 08110 901 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
39	JP 08095 786 A	<input checked="" type="checkbox"/>	ARITHMETIC PROCESSOR	

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40	JP 07210 323 A	<input checked="" type="checkbox"/>	DATA BATCH TRANSFER METHOD IN SEQUENTIAL ACCESS METHOD AND SECTION SEQUENTIAL ACCESS METHOD	
41	JP 07056 734 A	<input checked="" type="checkbox"/>	MICROPROCESSOR AND CONTROL METHOD THEREOF	
42	JP 06309 167 A	<input checked="" type="checkbox"/>	PROCESSOR FOR PARALLEL PROCESSING OF PLURAL INSTRUCTIONS	
43	JP 06242 954 A	<input checked="" type="checkbox"/>	METHOD FOR IMPROVING INSTRUCTION DISPATCH IN SUPERSCALAR PROCESSOR SYSTEM BY USING INDEPENDENTLY ACCESSED INTERMEDIATE STORAGE AREA AND SYSTEM FOR THE SAME	
44	JP 06236 275 A	<input checked="" type="checkbox"/>	METHOD AND SYSTEM FOR DISPATCHING AND EXECUTING NON-SEQUENTIAL INSTRUCTION IN A SUPERSCALAR PROCESSOR SYSTEM	
45	JP 06236 273 A	<input checked="" type="checkbox"/>	METHOD AND SYSTEM FOR DISPATCHING A PLURALITY OF INSTRUCTIONS BY ONE CYCLE IN SUPERSCALAR PROCESSOR SYSTEM	
46	JP 06236 267 A	<input checked="" type="checkbox"/>	METHOD AND SYSTEM FOR IMPROVING INSTRUCTION DISPATCHING EFFICIENCY IN SUPERSCALAR PROCESSOR	
47	JP 05324 477 A	<input checked="" type="checkbox"/>	ADDRESS TRANSFORMATION BUFFER MECHANISM	
48	JP 05313 894 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
49	JP 05233 229 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR AND INFORMATION PROCESSING METHOD	
50	JP 05224 921 A	<input checked="" type="checkbox"/>	DATA PROCESSING SYSTEM	
51	JP 05173 785 A	<input checked="" type="checkbox"/>	INSTRUCTION PREFETCHING DEVICE	
52	JP 05100 883 A	<input checked="" type="checkbox"/>	SEMICONDUCTOR DEVICE FOR PROCESSING DATA	
53	JP 05053 805 A	<input checked="" type="checkbox"/>	ELECTRONIC COMPUTER	
54	JP 04361 329 A	<input checked="" type="checkbox"/>	INSTRUCTION FETCH CIRCUIT	
55	JP 04326 127 A	<input checked="" type="checkbox"/>	PARALLEL INSTRUCTION EXECUTION SYSTEM	
56	JP 04175 930 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
57	JP 04153 733 A	<input checked="" type="checkbox"/>	INSTRUCTION SUPPLY DEVICE OF PARALLEL PROCESSOR	
58	JP 04116 727 A	<input checked="" type="checkbox"/>	INTERPRETER DEVICE	
59	JP 02289 097 A	<input checked="" type="checkbox"/>	METHOD AND DEVICE FOR PICTURE DISPLAY DATA PROCESSING	
60	JP 02280 247 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
61	JP 02257 342 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
62	JP 02236 657 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSING SYSTEM	

	Docum ent ID	U	Title	Current OR
63	JP 02118 833 A	<input checked="" type="checkbox"/>	INSTRUCTION DECODER	
64	JP 02112 054 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
65	JP 01292 437 A	<input checked="" type="checkbox"/>	DATA DRIVING TYPE CONTROL METHOD	
66	JP 01283 640 A	<input checked="" type="checkbox"/>	DATA DRIVING TYPE CONTROL METHOD	
67	JP 01126 733 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
68	JP 01123 549 A	<input checked="" type="checkbox"/>	PACKET SWITCH	
69	JP 01044 545 A	<input checked="" type="checkbox"/>	CENTRAL PROCESSING UNIT	
70	JP 63254 531 A	<input checked="" type="checkbox"/>	INSTRUCTION READ CONTROL SYSTEM FOR ELECTRONIC COMPUTER	
71	JP 63231 531 A	<input checked="" type="checkbox"/>	PIPELINE CONTROLLER	
72	JP 63201 832 A	<input checked="" type="checkbox"/>	PIPELINE PROCESSING TYPE INFORMATION PROCESSOR	
73	JP 63012 029 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
74	JP 62196 730 A	<input checked="" type="checkbox"/>	STAGE CONTROL SYSTEM FOR DATA PROCESSOR	
75	JP 62133 532 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
76	JP 62121 567 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
77	JP 61122 754 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
78	JP 60263 238 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
79	JP 60250 438 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
80	JP 60173 634 A	<input checked="" type="checkbox"/>	INSTRUCTION SIGNAL TRAIN PROCESSING CIRCUIT	
81	JP 60124 738 A	<input checked="" type="checkbox"/>	INITIAL SETTING AND DIAGNOSTIC CONTROLLING SYSTEM OF INFORMATION PROCESSING UNIT	
82	JP 58024 946 A	<input checked="" type="checkbox"/>	OPERATING PROCESSING SYSTEM	
83	JP 57103 553 A	<input checked="" type="checkbox"/>	INSTRUCTION READING SYSTEM	
84	JP 57029 154 A	<input type="checkbox"/>	INSTRUCTION BUFFER CONTROLLING SYSTEM	
85	JP 56162 151 A	<input type="checkbox"/>	INFORMATION PROCESSING DEVICE	

	Document ID	U	Title	Current OR
86	JP 54107 239 A	<input type="checkbox"/>	PROGRAM EXECUTION ORDER CONTROL SYSTEM	
87	EP 12514 25 A2	<input type="checkbox"/>	Very long instruction word information processing device and system	
88	EP 11071 11 A2	<input type="checkbox"/>	System and method for register renaming	
89	EP 11071 09 A2	<input type="checkbox"/>	Data processing device	
90	EP 10244 26 A2	<input type="checkbox"/>	High performance RISC microprocessor architecture	
91	EP 99289 4 A1	<input type="checkbox"/>	Apparatus and method for loop execution	
92	EP 99289 3 A1	<input type="checkbox"/>	Verifying instruction parallelism	
93	EP 88620 9 A2	<input type="checkbox"/>	Extensible risc microprocessor architecture	
94	EP 84966 5 A2	<input type="checkbox"/>	System and method for register renaming	
95	EP 74024 8 A1	<input type="checkbox"/>	Method and apparatus for detecting and executing traps in a superscalar processor	
96	EP 73791 5 A1	<input type="checkbox"/>	Method and apparatus for improving system performance in a data processing system	
97	EP 64448 2 A1	<input type="checkbox"/>	Dispatch of instructions to multiple execution units.	
98	WO 94163 84 A1	<input type="checkbox"/>	SYSTEM AND METHOD FOR REGISTER RENAMING	
99	EP 60664 3 A1	<input type="checkbox"/>	Method and system for nonsequential instruction dispatch and execution in a superscalar processor system.	
100	EP 60587 5 A1	<input type="checkbox"/>	Method and system for single cycle dispatch of multiple instruction in a superscalar processor system.	
101	EP 60586 8 A1	<input type="checkbox"/>	Method and system for indexing the assignment of intermediate storage buffers in a superscalar processor system.	
102	EP 60586 6 A1	<input type="checkbox"/>	Method and system for enhanced instruction dispatch in a superscalar processor system utilizing independently accessed intermediate storage.	
103	WO 93227 22 A1	<input type="checkbox"/>	A SYSTEM AND METHOD FOR RETIRING INSTRUCTIONS IN A SUPERSCALAR MICROPROCESSOR	
104	WO 93015 46 A1	<input type="checkbox"/>	EXTENSIBLE RISC MICROPROCESSOR ARCHITECTURE	
105	WO 93015 45 A1	<input type="checkbox"/>	HIGH-PERFORMANCE RISC MICROPROCESSOR ARCHITECTURE	
106	EP 47188 8 A2	<input type="checkbox"/>	Microprocessor for enhancing initiation of data processing after execution of conditional branch instruction.	
107	EP 44849 9 A2	<input type="checkbox"/>	Instruction prefetch method for branch-with-execute instructions.	
108	EP 30795 7 A2	<input type="checkbox"/>	Central processing unit having instruction prefetch function.	

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109	GB 20167 53 A	<input type="checkbox"/>	Data Processing System	
110	US 20030 13116 2 A	<input type="checkbox"/>	Non-destructive read FIFO memory device for multiple execution of instruction loops, has read pointer which is reset to address containing an instruction and then incremented to address of last instruction of loop	
111	JP 20031 86684 A	<input type="checkbox"/>	Dynamic waiting condition designation method of service logic program instance in intelligent network, involves designating maximum number of simultaneous execution of processes and length of waiting queue	
112	US 20030 06590 5 A	<input type="checkbox"/>	Parallel computation processor for high-speed loop operations has multiplexers which select either instructions dispatched from instruction dispatcher or instructions dispatched by instruction buffer operated by loop control unit	
113	US 64635 24 B	<input type="checkbox"/>	Multiple store instructions issuing method in superscalar data processing system, involves issuing selected address and data operands in single queue instruction slot to load/store and fixed point units, for execution	
114	WO 20024 6887 A	<input type="checkbox"/>	Concurrent multitasking processor for real-time operating system device, provides priority tags to instructions corresponding to selected tasks, in instruction queues and sends them to execution units	
115	US 63816 89 B	<input type="checkbox"/>	Superscalar microprocessor for computer system, has recorder buffer which allocates storage for instruction results corresponding to multiple concurrently dispatched instructions	
116	US 63246 40 B	<input type="checkbox"/>	Superscalar processor for use in data processing system, has delay register coupled to dispatch queue which dispatches several instruction groups and rename tables	
117	KR 20010 02485 A	<input type="checkbox"/>	Multi-thread microprocessor for instruction fetch	
118	EP 10508 05 A	<input type="checkbox"/>	Computer system for executing instructions with guard indicators, has supply circuit with main instruction queue to be supplied to parallel execution units and subsidiary instruction queue having priority access to execution pipelines	
119	US 61158 07 A	<input type="checkbox"/>	Static instruction decoder for superscalar processors, has timer indexed by pointer for indicating initial instruction to be issued in next clock cycle	
120	EP 99289 3 A	<input type="checkbox"/>	Processor for executing instructions in parallel has instruction buffer and decoders storing and decoding two instructions and arbitration and merge logic arbitrating between instructions	
121	WO 99576 38 A	<input type="checkbox"/>	Parallel data access method - involves buffering data submitted by sequence controller and instruction decoder during clock cycle, in respective register of processor, forwarding data to execution unit and combining them with corresponding commands	
122	US 58705 75 A	<input type="checkbox"/>	Guest branch instruction emulating method in data processing system e.g. desktop computer system	
123	US 58505 42 A	<input type="checkbox"/>	Cache system for fetching instructions in data processor - includes branch resolution unit that fetches non-guessed instruction stream corresponding to branch instruction and identification tag, during specified clock cycle	
124	GB 23243 92 A	<input type="checkbox"/>	Thread switch latency decreasing method for multithread processor - involves storing active threads in primary instruction queue for concurrent execution, and dormant threads in thread switch instruction queue for non-concurrent execution	
125	JP 10207 708 A	<input type="checkbox"/>	Programmable controller for control of industrial apparatus, machine, FA apparatus - executes succession instruction parallelly during multiple cycle instruction execution based on added two tags and buffer pointer	

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126	US 57873 03 A	<input type="checkbox"/>	Parallel processing system with arithmetic operation unit for executing very large instruction words - stops output of next VLIW from instruction buffer upon detection of no-operation state thereby delaying execution of next VLIW for instruction cycle	
127	JP 10105 399 A	<input type="checkbox"/>	Data processor with pipeline processing function - has instruction decoder that converts and outputs control signals of each function of pipeline, based on several simultaneously executable instructions detected from instruction buffer	
128	GB 23177 24 A	<input type="checkbox"/>	Multiple instruction parallel issue/execution management system - includes forward map buffer indicating whether instruction execution value result is to be used as input operand in other instruction	
129	JP 10003 425 A	<input type="checkbox"/>	Instruction input device for very long instruction word parallel computer - produces instruction code repeatedly with execution number, which is executed by parallel computer	
130	US 56175 49 A	<input type="checkbox"/>	Multiple instruction selection and buffering unit for CPU execution - has decoder generating bundle instruction indicating whether even and odd instruction pair can be executed simultaneously with selector routing instructions to operational units	
131	EP 82904 5 B	<input type="checkbox"/>	Method of rotating queued and fetched instructions for parallel processing in microprocessor - involves rotating all fetched and non-issued instructions together into issue order before next issue cycle.	
132	US 55420 58 A	<input type="checkbox"/>	Single chip CPU for pipelined processor - includes instruction queue to sequentially buffer operands during instruction decoding, then removing operands during instruction execution	
133	EP 69765 0 A	<input type="checkbox"/>	Instruction queue scanning for super-scalar CISC computer - using instruction cache feeding byte queue that is scanned to generate components relevant to each dispatch stage of RISC core processor	
134	EP 65132 1 A	<input type="checkbox"/>	Super-scalar microprocessor - decodes integer and floating point instructions in same microprocessor cycle and has common register file for accepting instruction results	
135	US 54817 43 A	<input type="checkbox"/>	Minimal instruction set computer system with multiple instruction issuing - has memory with bidirectional data port and instruction buffer for storing multiple instructions to be executed in parallel by multiple processing units	
136	EP 64686 1 B	<input type="checkbox"/>	History buffer system for allowing recovery of executed instructions - includes main history buffer with storage entries each having field for address of issued instruction, and tag field corresp. to subsidiary history buffer for storing control data	
137	EP 64448 2 A	<input type="checkbox"/>	Computer system for dispatching instructions to multiple execution units - defines instructions as dependent or independent for execution sequentially or in parallel depending upon definition and relationship to other instructions	
138	EP 63981 0 A	<input type="checkbox"/>	Temporary register storage for scalar processor - has multiple processors executing instructions and using rename buffers until control unit directs write back to general registers	
139	US 53353 30 A	<input type="checkbox"/>	Pipeline information processing appts. with reduced cycle time - adjusts program counter to enable use of otherwise idle buffer storage, so that instructions requiring multiple cycles can be processed in one cycle	
140	EP 68278 9 B	<input type="checkbox"/>	Register re-naming system for super-scalar reduced instruction set computers - assigns tag to each instruction in variable advance instruction window and stores results of instructions executed in buffer according to corresp tags	
141	EP 60586 8 A	<input type="checkbox"/>	Instruction dispatching method for super-scalar processor system - involves using storage buffers for instructions which are dispatched between time that storage buffer has been assigned for specific general register and results of execution are moved	

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142	EP 66308 3 B	<input type="checkbox"/>	Load and store operation handling for superscalar processors - has load and store unit handling out of order requests, address collision detection and data alignment of eight unaligned data bytes	
143	EP 63818 3 B	<input type="checkbox"/>	Retiring instructions in superscalar microprocessor - stores results of incomplete instructions in temporary registers and retires instructions when their results can be moved to register array	
144	EP 55117 3 A	<input type="checkbox"/>	Dataflow architecture for computer - executes instructions according to instruction queue on outside and active operands and stores results as next active operand	
145	US 52127 79 A	<input type="checkbox"/>	Pipelined data processor for executing processing instruction in parallel - has number of microprograms stored in microprogram memory, microprogram counter, instruction decoding and executing stages and store buffer and selector	
146	US 52010 57 A	<input type="checkbox"/>	Central processing unit for computer - has instruction queue for storing series of instructions and processing elements for executing instructions and sink matrix storing results of execution of multiple interactions of instructions	
147	US 51858 68 A	<input type="checkbox"/>	Computer instruction executing appts. with pipelined architecture - sends instructions to executing unit according to logical sequence and shifts other instructions into vacant decoders	
148	EP 52057 2 A	<input type="checkbox"/>	Data processing appts. - uses single instruction with FIFO buffer to distribute operating codes to multiple processors	
149	EP 51842 0 A	<input type="checkbox"/>	Computer system with multiple duplicate functional units for concurrent processing - has instruction issue unit with register files coupled by interconnection network to main memory and cache memory, to process out-of-order instructions	
150	DE 42112 22 A	<input type="checkbox"/>	Branch instruction target controller for super-scaling processor system - has branch target buffer providing tabulated group of instructions with instruction checking unit	
151	GB 22508 40 A	<input type="checkbox"/>	Extended branch target logic for microprocessor - executes branch instruction and is target instruction stored in branch target buffer to be executed concurrently, minimising delay in pipeline processor	
152	EP 45326 8 A	<input type="checkbox"/>	Microprocessor for inserting bus cycle to output internal information - has bus controller coupled to other processors to enable insertion of bus cycle in accordance with bus cycle request signal	
153	US 52261 30 A	<input type="checkbox"/>	Branch prediction cache with maintained consistency - organises store into instruction stream detection resulting in invalidation of corresponding cache entry data and main memory access	
154	EP 43803 8 B	<input type="checkbox"/>	Graphic processor for picture screen - converts general graphic instructions to sequence of primitive pixel orientated instructions for storage in queue memory	
155	EP 41343 4 A	<input type="checkbox"/>	Pipelined processor with variable instruction length - has latch circuit holding instruction preceding each instruction memory access to quickly provide variable length instructions	
156	EP 38147 1 A	<input type="checkbox"/>	Multiple instruction pre-processor - resolves data dependencies during pre-processing of multiple instructions prior to execution of those instructions in digital computer	
157	EP 38085 9 A	<input type="checkbox"/>	Source list, pointer queues and result queues - resolving data dependency during pre-processing of multiple instructions prior to execution of those instructions in digital computer	
158	EP 36055 3 A	<input type="checkbox"/>	Write-back system maintaining identity between buffer and main store - has duplicated buffer store and move-out buffers arranged to transfer two halves of data concurrently	
159	AU 88234 38 A	<input type="checkbox"/>	Prefetching queue control system - has instruction read out from memory and stored in buffer with write and transfer devices for prefetching parallel to instruction execution	
160	US 48169 91 A	<input type="checkbox"/>	VM system for holding host and multiple guest entries - has address translation look-aside buffer, and instruction execution unit to command start by setting CPU to necessary fields of guest	

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161	EP 26826 4 A	<input type="checkbox"/>	High speed pipelined - indicates when control instruction is decoded and serialisation element is to be input to necessary units	
162	US 47362 92 A	<input type="checkbox"/>	Electronic data processing method overlaid jump insertion - having jump target instruction and corresp. control word portion concurrently written over instruction	
163	EP 23909 7 A	<input type="checkbox"/>	Data processing system with decoded instruction queue memory - has queue structure composed of entries for latching entry information and including up-down counter	
164	EP 23908 1 A	<input type="checkbox"/>	Pipelined data processor for parallel processing - has pair of instruction registers storing two instructions to be executed	
165	DE 35862 35 G	<input type="checkbox"/>	Instruction prefetch operation for branch instructions - by generating control tag whose current value is changed each time branch instruction is reached	
166	US 45610 52 A	<input type="checkbox"/>	Instruction pre-fetch system for pipelining information processor - has control logic that moves instruction addresses through selector, instruction buffer and logical and physical address generator	
167	EP 11882 8 A	<input type="checkbox"/>	Instruction fetch look-aside buffer for data processing. - reduces fetches from storage under loop mode control by extracting instructions directly from the buffer	
168	EP 10833 8 A	<input type="checkbox"/>	Parallel queuing method for multiprocessor data processing system - providing lock for de-queuing any element and which is examined by that program routine to delete but not insert anchor-pointed element	
169	EP 10667 0 A	<input type="checkbox"/>	Digital data processor with multiple execution units - has operation code identifying each instruction issued in program order to queue of collector, and results stored in stack	
170	DE 32471 96 A	<input type="checkbox"/>	Microprocessor operating system - provides simultaneous execution of multiple programs so that programs are polled successively and instructions and data are queued	
171	EP 36093 A	<input type="checkbox"/>	Information processing system with single chip arithmetic control unit - preventing malfunction by rendering content of instruction buffers ineffective and rewritten under certain conditions	

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1	US 20040 05487 2 A1	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/206
2	US 20040 04487 8 A1	<input checked="" type="checkbox"/>	Synchronisation between pipelines in a data processing apparatus	712/34
3	US 20040 00321 6 A1	<input checked="" type="checkbox"/>	Branch prediction apparatus and method	712/237
4	US 20030 18813 9 A1	<input checked="" type="checkbox"/>	Flexible demand-based resource allocation for multiple requestors in a simultaneous multi-threaded CPU	712/225
5	US 20030 16367 1 A1	<input checked="" type="checkbox"/>	Method and apparatus for prioritized instruction issue queue	712/214
6	US 20030 12090 0 A1	<input checked="" type="checkbox"/>	Apparatus and method for a software pipeline loop procedure in a digital signal processor	712/215
7	US 20030 11020 1 A1	<input checked="" type="checkbox"/>	VLIW instruction control	718/102
8	US 20030 07911 3 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/205
9	US 20030 07454 6 A1	<input checked="" type="checkbox"/>	Data processing apparatus	712/241
10	US 20030 07006 0 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
11	US 20030 06590 5 A1	<input checked="" type="checkbox"/>	Parallel computation processor, parallel computation control method and program thereof	712/23
12	US 20030 05608 7 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
13	US 20030 05608 6 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
14	US 20030 04315 6 A1	<input checked="" type="checkbox"/>	Apparatus and method for extracting and loading data to/from a buffer	345/537
15	US 20030 04081 4 A1	<input checked="" type="checkbox"/>	Method for controlling mechanisms and technical systems a corresponding device and control software	700/42
16	US 20030 03924 8 A1	<input checked="" type="checkbox"/>	System and method for the consolidation of data packets	370/392
17	US 20020 17438 5 A1	<input checked="" type="checkbox"/>	Computer system with debug facility	714/38

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18	US 20020 15699 2 A1	<input checked="" type="checkbox"/>	Information processing device and computer system	712/24
19	US 20020 02932 8 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
20	US 20010 04977 0 A1	<input checked="" type="checkbox"/>	BUFFER MEMORY MANAGEMENT IN A SYSTEM HAVING MULTIPLE EXECUTION ENTITIES	711/129
21	US 20010 04219 2 A1	<input checked="" type="checkbox"/>	Mechanism for self-initiated instruction issuing and method therefor	712/215
22	US 20010 02523 7 A1	<input checked="" type="checkbox"/>	Computer system with debug facility	703/26
23	US 66717 94 B1	<input checked="" type="checkbox"/>	Address generation interlock detection	712/217
24	US 66657 96 B1	<input checked="" type="checkbox"/>	Microprocessor instruction result obfuscation	713/190
25	US 66314 59 B1	<input checked="" type="checkbox"/>	Extended instruction word folding apparatus	712/210
26	US 66092 47 B1	<input checked="" type="checkbox"/>	Method and apparatus for re-creating the trace of an emulated instruction set when executed on hardware native to a different instruction set field	717/128
27	US 65981 52 B1	<input checked="" type="checkbox"/>	Increasing the overall prediction accuracy for multi-cycle branch prediction and apparatus by enabling quick recovery	712/228
28	US 65052 95 B1	<input checked="" type="checkbox"/>	Data processor	712/241
29	US 63306 57 B1	<input checked="" type="checkbox"/>	Pairing of micro instructions in the instruction queue	712/23
30	US 63082 60 B1	<input checked="" type="checkbox"/>	Mechanism for self-initiated instruction issuing and method therefor	712/215
31	US 63026 98 B1	<input checked="" type="checkbox"/>	Method and apparatus for on-line teaching and learning	434/323
32	US 62956 00 B1	<input checked="" type="checkbox"/>	Thread switch on blocked load or store using instruction thread field	712/228
33	US 62470 64 B1	<input checked="" type="checkbox"/>	Enqueue instruction in a system architecture for improved message passing and process synchronization	719/312
34	US 62090 81 B1	<input checked="" type="checkbox"/>	Method and system for nonsequential instruction dispatch and execution in a superscalar processor system	712/215
35	US 61087 66 A	<input checked="" type="checkbox"/>	Structure of processor having a plurality of main processors and sub processors, and a method for sharing the sub processors	712/34
36	US 60818 87 A	<input checked="" type="checkbox"/>	System for passing an index value with each prediction in forward direction to enable truth predictor to associate truth value with particular branch instruction	712/239
37	US 60386 53 A	<input checked="" type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
38	US 59564 95 A	<input checked="" type="checkbox"/>	Method and system for processing branch instructions during emulation in a data processing system	703/26

	Docum ent ID	U	Title	Current OR
39	US 59419 84 A	<input checked="" type="checkbox"/>	Data processing device	712/218
40	US 59207 10 A	<input checked="" type="checkbox"/>	Apparatus and method for modifying status bits in a reorder buffer with a large speculative state	712/216
41	US 59037 41 A	<input checked="" type="checkbox"/>	Method of allocating a fixed reorder buffer storage line for execution results regardless of a number of concurrently dispatched instructions	712/218
42	US 58988 82 A	<input checked="" type="checkbox"/>	Method and system for enhanced instruction dispatch in a superscalar processor system utilizing independently accessed intermediate storage	712/23
43	US 58945 82 A	<input checked="" type="checkbox"/>	Method of controlling parallel processing at an instruction level and processor for realizing the method	712/23
44	US 58945 75 A	<input checked="" type="checkbox"/>	Method and system for initial state determination for instruction trace reconstruction	717/128
45	US 58705 79 A	<input checked="" type="checkbox"/>	Reorder buffer including a circuit for selecting a designated mask corresponding to an instruction that results in an exception	712/217
46	US 58705 75 A	<input checked="" type="checkbox"/>	Indirect unconditional branches in data processing system emulation mode	712/209
47	US 57846 04 A	<input checked="" type="checkbox"/>	Method and system for reduced run-time delay during conditional branch execution in pipelined processor systems utilizing selectively delayed sequential instruction purging	712/238
48	US 56757 76 A	<input checked="" type="checkbox"/>	Data processor using FIFO memories for routing operations to parallel operational units	712/220
49	US 55749 39 A	<input checked="" type="checkbox"/>	Multiprocessor coupling system with integrated compile and run time scheduling for parallelism	712/24
50	US 54918 29 A	<input checked="" type="checkbox"/>	Method and system for indexing the assignment of intermediate storage buffers in a superscalar processor system	712/23
51	US 54653 73 A	<input checked="" type="checkbox"/>	Method and system for single cycle dispatch of multiple instructions in a superscalar processor system	712/215
52	US 54653 72 A	<input checked="" type="checkbox"/>	Dataflow computer for following data dependent path processes	712/25
53	US 54524 27 A	<input checked="" type="checkbox"/>	Data processing device for variable word length instruction system having short instruction execution time and small occupancy area	712/210
54	US 54370 17 A	<input checked="" type="checkbox"/>	Method and system for maintaining translation lookaside buffer coherency in a multiprocessor data processing system	709/213
55	US 54044 71 A	<input checked="" type="checkbox"/>	Method and apparatus for switching address generation modes in CPU having plural address generation modes	712/207
56	US 53815 32 A	<input checked="" type="checkbox"/>	Microprocessor having branch aligner between branch buffer and instruction decoder unit for enhancing initiation of data processing after execution of conditional branch instruction	712/237
57	US 53496 56 A	<input checked="" type="checkbox"/>	Task scheduling method in a multiprocessor system where task selection is determined by processor identification and evaluation information	718/102
58	US 53353 30 A	<input checked="" type="checkbox"/>	Information processing apparatus with optimization programming	712/241
59	US 48932 33 A	<input checked="" type="checkbox"/>	Method and apparatus for dynamically controlling each stage of a multi-stage pipelined data unit	712/244
60	US 47665 66 A	<input checked="" type="checkbox"/>	Performance enhancement scheme for a RISC type VLSI processor using dual execution units for parallel instruction processing	712/23
61	US 45610 52 A	<input checked="" type="checkbox"/>	Instruction prefetch system	712/207

	Docum ent ID	U	Title	Current OR
62	US 45325 89 A	<input checked="" type="checkbox"/>	Digital data processor with two operation units	712/217
63	US 42311 06 A	<input checked="" type="checkbox"/>	Performance monitor apparatus and method	702/186
64	US 42009 27 A	<input checked="" type="checkbox"/>	Multi-instruction stream branch processing mechanism	712/235
65	US 41722 84 A	<input type="checkbox"/>	Priority interrupt apparatus employing a plural stage shift register having separate interrupt mechanisms coupled to the different stages thereof for segregating interrupt requests according to priority levels	710/264

	Docum ent ID	U	Title	Current OR
1	JP 20023 18687 A	<input type="checkbox"/>	INFORMATION PROCESSOR AND COMPUTER SYSTEM	
2	JP 20020 41284 A	<input checked="" type="checkbox"/>	DEVICE FOR CONTRACTING EXTENDED INSTRUCTION WORD	
3	JP 20023 18687 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR AND COMPUTER SYSTEM	
4	JP 20020 41284 A	<input checked="" type="checkbox"/>	DEVICE FOR CONTRACTING EXTENDED INSTRUCTION WORD	
5	JP 20001 81709 A	<input checked="" type="checkbox"/>	INSTRUCTION CONTROLLER	
6	JP 10091 436 A	<input checked="" type="checkbox"/>	PROGRAM LOADER	
7	JP 09198 374 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	
8	JP 08055 026 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
9	JP 06332 701 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
10	JP 06236 275 A	<input checked="" type="checkbox"/>	METHOD AND SYSTEM FOR DISPATCHING AND EXECUTING NON-SEQUENTIAL INSTRUCTION IN A SUPERSCALAR PROCESSOR SYSTEM	
11	JP 06236 267 A	<input checked="" type="checkbox"/>	METHOD AND SYSTEM FOR IMPROVING INSTRUCTION DISPATCHING EFFICIENCY IN SUPERSCALAR PROCESSOR	
12	JP 06161 745 A	<input checked="" type="checkbox"/>	METHOD AND DEVICE FOR VERIFYING DATA PROCESSOR	
13	JP 03188 530 A	<input checked="" type="checkbox"/>	PROGRAM PREFETCHING DEVICE	
14	JP 02118 833 A	<input checked="" type="checkbox"/>	INSTRUCTION DECODER	
15	JP 62031 439 A	<input checked="" type="checkbox"/>	INSTRUCTION REPROCESSING CONTROL SYSTEM	
16	JP 60263 238 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
17	JP 60124 738 A	<input checked="" type="checkbox"/>	INITIAL SETTING AND DIAGNOSTIC CONTROLLING SYSTEM OF INFORMATION PROCESSING UNIT	
18	EP 12514 25 A2	<input checked="" type="checkbox"/>	Very long instruction word information processing device and system	
19	EP 60587 5 A1	<input checked="" type="checkbox"/>	Method and system for single cycle dispatch of multiple instruction in a superscalar processor system.	
20	EP 60586 8 A1	<input checked="" type="checkbox"/>	Method and system for indexing the assignment of intermediate storage buffers in a superscalar processor system.	
21	EP 60586 6 A1	<input checked="" type="checkbox"/>	Method and system for enhanced instruction dispatch in a superscalar processor system utilizing independently accessed intermediate storage.	

	Docum ent ID	U	Title	Current OR
22	EP 47188 8 A2	<input checked="" type="checkbox"/>	Microprocessor for enhancing initiation of data processing after execution of conditional branch instruction.	
23	US 20030 06590 5 A	<input checked="" type="checkbox"/>	Parallel computation processor for high-speed loop operations has multiplexers which select either instructions dispatched from instruction dispatcher or instructions dispatched by instruction buffer operated by loop control unit	
24	EP 12514 25 A	<input checked="" type="checkbox"/>	Information processor e.g. computer system has controller which selects predetermined number of instructions from instruction buffer, and transmits to another buffer for executing instructions in parallel	
25	WO 20024 6887 A	<input checked="" type="checkbox"/>	Concurrent multitasking processor for real-time operating system device, provides priority tags to instructions corresponding to selected tasks, in instruction queues and sends them to execution units	
26	US 58705 75 A	<input checked="" type="checkbox"/>	Guest branch instruction emulating method in data processing system e.g. desktop computer system	
27	GB 23243 92 A	<input checked="" type="checkbox"/>	Thread switch latency decreasing method for multithread processor - involves storing active threads in primary instruction queue for concurrent execution, and dormant threads in thread switch instruction queue for non-concurrent execution	
28	US 53353 30 A	<input checked="" type="checkbox"/>	Pipeline information processing appts. with reduced cycle time - adjusts program counter to enable use of otherwise idle buffer storage, so that instructions requiring multiple cycles can be processed in one cycle	
29	US 52631 69 A	<input checked="" type="checkbox"/>	Bus arbitration and re source management for signal processor - has processor arbiter which supervises on priority basis both captive processor resources and independent processor resources	
30	EP 55117 3 A	<input checked="" type="checkbox"/>	Dataflow architecture for computer - executes instructions according to instruction queue on outside and active operands and stores results as next active operand	
31	EP 52057 2 A	<input checked="" type="checkbox"/>	Data processing appts. - uses single instruction with FIFO buffer to distribute operating codes to multiple processors	
32	GB 22508 40 A	<input checked="" type="checkbox"/>	Extended branch target logic for microprocessor - executes branch instruction and is target instruction stored in branch target buffer to be executed concurrently, minimising delay in pipeline processor	
33	EP 41343 4 A	<input checked="" type="checkbox"/>	Pipelined processor with variable instruction length - has latch circuit holding instruction preceding each instruction memory access to quickly provide variable length instructions	
34	BR 88049 69 A	<input checked="" type="checkbox"/>	Multiple instruction stream multiple data pipelined processing appts. - includes pipelined processors connected to receiver for temporarily holding incoming instructions	
35	EP 23908 1 A	<input checked="" type="checkbox"/>	Pipelined data processor for parallel processing - has pair of instruction registers storing two instructions to be executed	
36	US 45610 52 A	<input checked="" type="checkbox"/>	Instruction pre-fetch system for pipelining information processor - has control logic that moves instruction addresses through selector, instruction buffer and logical and physical address generator	
37	DE 32471 96 A	<input type="checkbox"/>	Microprocessor operating system - provides simultaneous execution of multiple programs so that programs are polled successively and instructions and data are queued	

	Docum ent ID	U	Title	Current OR
1	US 20040 06465 3 A1	<input type="checkbox"/>	System and method for limited fanout daisy chaining of cache invalidation requests in a shared-memory multiprocessor system	711/145
2	US 20030 18251 1 A1	<input checked="" type="checkbox"/>	Apparatus and method for resolving an instruction conflict in a software pipeline nested loop procedure in a digital signal processor	711/125
3	US 20030 15901 9 A1	<input checked="" type="checkbox"/>	Prediction of instructions in a data processing apparatus	712/207
4	US 20030 15446 9 A1	<input checked="" type="checkbox"/>	Apparatus and method for improved execution of a software pipeline loop procedure in a digital signal processor	717/161
5	US 20030 12090 5 A1	<input checked="" type="checkbox"/>	Apparatus and method for executing a nested loop program with a software pipeline loop procedure in a digital signal processor	712/241
6	US 20030 12089 9 A1	<input checked="" type="checkbox"/>	Apparatus and method for processing an interrupt in a software pipeline loop procedure in a digital signal processor	712/214
7	US 20030 12088 2 A1	<input checked="" type="checkbox"/>	Apparatus and method for exiting from a software pipeline loop procedure in a digital signal processor	711/169
8	US 20030 03454 4 A1	<input checked="" type="checkbox"/>	Microcomputer	257/523
9	US 20030 01622 4 A1	<input checked="" type="checkbox"/>	Display apparatus in which recovery time is short in fault occurrence	345/506
10	US 20020 19908 3 A1	<input checked="" type="checkbox"/>	High code-density microcontroller architecture with changeable instruction formats	712/209
11	US 20020 18447 9 A1	<input checked="" type="checkbox"/>	Bytecode instruction processor with switch instruction handling logic	712/236
12	US 20020 12920 8 A1	<input checked="" type="checkbox"/>	System for handling coherence protocol races in a scalable shared memory system based on chip multiprocessing	711/141
13	US 20020 12414 4 A1	<input checked="" type="checkbox"/>	Scalable multiprocessor system and cache coherence method implementing store-conditional memory transactions while an associated directory entry is encoded as a coarse bit vector	711/145
14	US 20020 12414 3 A1	<input checked="" type="checkbox"/>	System and method for generating cache coherence directory entries and error correction codes in a multiprocessor system	711/145
15	US 20020 11212 2 A1	<input checked="" type="checkbox"/>	Verifying cumulative ordering	711/119
16	US 20020 08780 7 A1	<input checked="" type="checkbox"/>	System for minimizing directory information in scalable multiprocessor systems with logically independent input/output nodes	711/141
17	US 20020 08780 6 A1	<input checked="" type="checkbox"/>	Cache coherence protocol engine and method for efficient processing of interleaved memory transactions in a multiprocessor system	711/141

	Docum ent ID	U	Title	Current OR
18	US 20020 08327 4 A1	<input checked="" type="checkbox"/>	Scalable multiprocessor system and cache coherence method incorporating invalid-to-dirty requests	711/144
19	US 20020 04632 7 A1	<input checked="" type="checkbox"/>	Cache coherence protocol engine and method for processing memory transaction in distinct address subsets during interleaved time periods in a multiprocessor system	711/141
20	US 20020 02044 4 A1	<input checked="" type="checkbox"/>	Automatically switching valve with remote signaling	137/112
21	US 20020 01690 3 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
22	US 20020 01084 0 A1	<input checked="" type="checkbox"/>	Multiprocessor cache coherence system and method in which processor nodes and input/output nodes are equal participants	711/141
23	US 20020 00744 3 A1	<input checked="" type="checkbox"/>	Scalable multiprocessor system and cache coherence method	711/141
24	US 20020 00743 9 A1	<input checked="" type="checkbox"/>	System and method for limited fanout daisy chaining of cache invalidation requests in a shared-memory multiprocessor system	711/119
25	US 20010 03230 7 A1	<input checked="" type="checkbox"/>	MICRO-INSTRUCTION QUEUE FOR A MICROPROCESSOR INSTRUCTION PIPELINE	712/219
26	US 20010 02751 3 A1	<input checked="" type="checkbox"/>	Parallel processor and image processing system using the processor	712/22
27	US 67082 96 B1	<input checked="" type="checkbox"/>	Method and system for selecting and distinguishing an event sequence using an effective address in a processing system	714/47
28	US 67014 84 B1	<input checked="" type="checkbox"/>	Register file with delayed parity check	714/801
29	US 66979 19 B2	<input checked="" type="checkbox"/>	System and method for limited fanout daisy chaining of cache invalidation requests in a shared-memory multiprocessor system	711/141
30	US 66752 65 B2	<input checked="" type="checkbox"/>	Multiprocessor cache coherence system and method in which processor nodes and input/output nodes are equal participants	711/141
31	US 66402 87 B2	<input checked="" type="checkbox"/>	Scalable multiprocessor system and cache coherence method incorporating invalid-to-dirty requests	711/141
32	US 66369 49 B2	<input checked="" type="checkbox"/>	System for handling coherence protocol races in a scalable shared memory system based on chip multiprocessing	711/141
33	US 66257 56 B1	<input checked="" type="checkbox"/>	Replay mechanism for soft error recovery	714/17
34	US 66222 36 B1	<input checked="" type="checkbox"/>	Microprocessor instruction fetch unit for processing instruction groups having multiple branch instructions	712/206
35	US 66222 18 B2	<input checked="" type="checkbox"/>	Cache coherence protocol engine and method for efficient processing of interleaved memory transactions in a multiprocessor system	711/141
36	US 66222 17 B2	<input checked="" type="checkbox"/>	Cache coherence protocol engine system and method for processing memory transaction in distinct address subsets during interleaved time periods in a multiprocessor system	711/141
37	US 66112 69 B1	<input checked="" type="checkbox"/>	Video display unit and program recording medium	345/522

	Docum ent ID	U	Title	Current OR
38	US 65781 34 B1	<input checked="" type="checkbox"/>	Multi-branch resolution	712/219
39	US 65606 95 B1	<input checked="" type="checkbox"/>	Dynamic pipe staging adder	712/214
40	US 65364 56 B2	<input checked="" type="checkbox"/>	Automatically switching valve with remote signaling	137/12
41	US 65295 09 B1	<input checked="" type="checkbox"/>	Switch controlling apparatus for small capacitance ATM exchange	370/395 .4
42	US 64991 16 B1	<input checked="" type="checkbox"/>	Performance of data stream touch events	714/39
43	US 64842 56 B1	<input checked="" type="checkbox"/>	Apparatus and method of branch prediction utilizing a comparison of a branch history table to an aliasing table	712/240
44	US 64776 54 B1	<input checked="" type="checkbox"/>	Managing VT for reduced power using power setting commands in the instruction stream	713/300
45	US 64497 10 B1	<input checked="" type="checkbox"/>	Stitching parcels	712/216
46	US 64143 68 B1	<input checked="" type="checkbox"/>	Microcomputer with high density RAM on single chip	257/523
47	US 64120 64 B1	<input checked="" type="checkbox"/>	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
48	US 63517 96 B1	<input checked="" type="checkbox"/>	Methods and apparatus for increasing the efficiency of a higher level cache by selectively performing writes to the higher level cache	711/204
49	US 63341 84 B1	<input checked="" type="checkbox"/>	Processor and method of fetching an instruction that select one of a plurality of decoded fetch addresses generated in parallel to form a memory request	712/235
50	US 63112 67 B1	<input checked="" type="checkbox"/>	Just-in-time register renaming technique	712/217
51	US 62826 30 B1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
52	US 62759 03 B1	<input checked="" type="checkbox"/>	Stack cache miss handling	711/132
53	US 62667 67 B1	<input checked="" type="checkbox"/>	Apparatus and method for facilitating out-of-order execution of load instructions	712/217
54	US 62667 61 B1	<input checked="" type="checkbox"/>	Method and system in an information processing system for efficient maintenance of copies of values stored within registers	712/23
55	US 62498 55 B1	<input checked="" type="checkbox"/>	Arbiter system for central processing unit having dual dominoed encoders for four instruction issue per machine cycle	712/23
56	US 62405 10 B1	<input checked="" type="checkbox"/>	System for processing a cluster of instructions where the instructions are issued to the execution units having a priority order according to a template associated with the cluster of instructions	712/236
57	US 62370 86 B1	<input checked="" type="checkbox"/>	1 Method to prevent pipeline stalls in superscalar stack based computing systems	712/226
58	US 62370 77 B1	<input checked="" type="checkbox"/>	Instruction template for efficient processing clustered branch instructions	712/24
59	US 62162 06 B1	<input checked="" type="checkbox"/>	Trace victim cache	711/133

	Docum ent ID	U	Title	Current OR
60	US 62126 19 B1	<input checked="" type="checkbox"/>	System and method for high-speed register renaming by counting	712/23
61	US 62090 73 B1	<input checked="" type="checkbox"/>	System and method for interlocking barrier operations in load and store queues	711/169
62	US 61890 72 B1	<input checked="" type="checkbox"/>	Performance monitoring of cache misses and instructions completed for instruction parallelism analysis	711/118
63	US 61700 50 B1	<input checked="" type="checkbox"/>	Length decoder for variable length data	712/210
64	US 61700 38 B1	<input checked="" type="checkbox"/>	Trace based instruction caching	711/125
65	US 61311 57 A	<input checked="" type="checkbox"/>	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
66	US 61287 20 A	<input checked="" type="checkbox"/>	Distributed processing array with component processors performing customized interpretation of instructions	712/20
67	US 61087 68 A	<input checked="" type="checkbox"/>	Reissue logic for individually reissuing instructions trapped in a multiissue stack based computing system	712/214
68	US 61051 28 A	<input checked="" type="checkbox"/>	Method and apparatus for dispatching instructions to execution units in waves	712/215
69	US 60853 38 A	<input checked="" type="checkbox"/>	CPI infinite and finite analysis	714/47
70	US 60790 02 A	<input checked="" type="checkbox"/>	Dynamic expansion of execution pipeline stages	711/169
71	US 60761 44 A	<input checked="" type="checkbox"/>	Method and apparatus for identifying potential entry points into trace segments	711/125
72	US 60732 13 A	<input checked="" type="checkbox"/>	Method and apparatus for caching trace segments with multiple entry points	711/125
73	US 60613 67 A	<input checked="" type="checkbox"/>	Processor with pipelining structure and method for high-speed calculation with pipelining processors	370/535
74	US 60498 82 A	<input checked="" type="checkbox"/>	Apparatus and method for reducing power consumption in a self-timed system	713/322
75	US 60411 67 A	<input checked="" type="checkbox"/>	Method and system for reordering instructions after dispatch in a processing system	712/214
76	US 60290 06 A	<input checked="" type="checkbox"/>	Data processor with circuit for regulating instruction throughput while powered and method of operation	713/323
77	US 60237 56 A	<input checked="" type="checkbox"/>	Instruction processing method and system for variable-length instructions	712/208
78	US 60212 61 A	<input checked="" type="checkbox"/>	Method and system for testing a multiprocessor data processing system utilizing a plurality of event tracers	714/37
79	US 60187 86 A	<input checked="" type="checkbox"/>	Trace based instruction caching	711/4
80	US 60063 09 A	<input checked="" type="checkbox"/>	Information block transfer management in a multiprocessor computer system employing private caches for individual center processor units and a shared cache	711/123
81	US 59876 16 A	<input checked="" type="checkbox"/>	Semiconductor device	713/320
82	US 59788 96 A	<input checked="" type="checkbox"/>	Method and system for increased instruction dispatch efficiency in a superscalar processor system	712/23

	Docum ent ID	U	Title	Current OR
83	US 59745 35 A	<input checked="" type="checkbox"/>	Method and system in data processing system of permitting concurrent processing of instructions of a particular type	712/215
84	US 59704 39 A	<input checked="" type="checkbox"/>	Performance monitoring in a data processing system	702/186
85	US 59639 73 A	<input checked="" type="checkbox"/>	Multiprocessor computer system incorporating method and apparatus for dynamically assigning ownership of changeable data	711/130
86	US 59616 54 A	<input checked="" type="checkbox"/>	Operand fetch bandwidth analysis	714/47
87	US 59580 41 A	<input checked="" type="checkbox"/>	Latency prediction in a pipelined microarchitecture	712/214
88	US 59516 79 A	<input checked="" type="checkbox"/>	Microprocessor circuits, systems, and methods for issuing successive iterations of a short backward branch loop in a single cycle	712/241
89	US 59499 71 A	<input checked="" type="checkbox"/>	Method and system for performance monitoring through identification of frequency and length of time of execution of serialization instructions in a processing system	714/47
90	US 59419 62 A	<input checked="" type="checkbox"/>	Buffer management system for releasing a buffer area based on holding time and maximum allowable time when remaining buffer areas reached threshold	710/53
91	US 59387 60 A	<input checked="" type="checkbox"/>	System and method for performance monitoring of instructions in a re-order buffer	712/220
92	US 59305 08 A	<input checked="" type="checkbox"/>	Method for storing and decoding instructions for a microprocessor having a plurality of function units	717/158
93	US 59304 95 A	<input checked="" type="checkbox"/>	Method and system for processing a first instruction in a first processing environment in response to initiating processing of a second instruction in a emulation environment	703/26
94	US 59283 55 A	<input checked="" type="checkbox"/>	Apparatus for reducing instruction issue stage stalls through use of a staging register	712/214
95	US 59251 22 A	<input checked="" type="checkbox"/>	Data processing unit which pre-fetches instructions of different lengths to conduct processing	712/210
96	US 59220 69 A	<input checked="" type="checkbox"/>	Reorder buffer which forwards operands independent of storing destination specifiers therein	712/217
97	US 59220 68 A	<input checked="" type="checkbox"/>	Information processing system and information processing method for executing instructions in parallel	712/215
98	US 59180 34 A	<input checked="" type="checkbox"/>	Method for decoupling pipeline stages	712/218
99	US 59130 54 A	<input checked="" type="checkbox"/>	Method and system for processing a multiple-register instruction that permit multiple data words to be written in a single processor cycle	712/220
100	US 59060 02 A	<input checked="" type="checkbox"/>	Method and apparatus for saving and restoring the context of registers using different instruction sets for different sized registers	711/171
101	US 59000 25 A	<input checked="" type="checkbox"/>	Processor having a hierarchical control register file and methods for operating the same	712/248
102	US 59000 12 A	<input checked="" type="checkbox"/>	Storage device having varying access times and a superscalar microprocessor employing the same	711/120
103	US 58988 52 A	<input checked="" type="checkbox"/>	Load instruction steering in a dual data cache microarchitecture	712/214
104	US 58976 55 A	<input checked="" type="checkbox"/>	System and method for cache replacement within a cache set based on valid, modified or least recently used status in order of preference	711/134
105	US 58954 86 A	<input checked="" type="checkbox"/>	Method and system for selectively invalidating cache lines during multiple word store operations for memory coherence	711/121

	Docum ent ID	U	Title	Current OR
106	US 58813 06 A	<input checked="" type="checkbox"/>	Instruction fetch bandwidth analysis	712/23
107	US 58782 08 A	<input checked="" type="checkbox"/>	Method and system for instruction trace reconstruction utilizing limited output pins and bus monitoring	714/38
108	US 58706 16 A	<input checked="" type="checkbox"/>	System and method for reducing power consumption in an electronic circuit	713/324
109	US 58706 12 A	<input checked="" type="checkbox"/>	Method and apparatus for condensed history buffer	710/260
110	US 58705 82 A	<input checked="" type="checkbox"/>	Method and apparatus for completion of non-interruptible instructions before the instruction is dispatched	712/218
111	US 58705 80 A	<input checked="" type="checkbox"/>	Decoupled forwarding reorder buffer configured to allocate storage in chunks for instructions having unresolved dependencies	712/218
112	US 58623 71 A	<input checked="" type="checkbox"/>	Method and system for instruction trace reconstruction utilizing performance monitor outputs and bus monitoring	712/228
113	US 58600 26 A	<input checked="" type="checkbox"/>	Information processing system for controlling operations of input/output devices of another clusters according to control instructions issued from a cluster	710/33
114	US 58600 14 A	<input checked="" type="checkbox"/>	Method and apparatus for improved recovery of processor state using history buffer	710/260
115	US 58451 06 A	<input checked="" type="checkbox"/>	Method for simulating cache operation	703/21
116	US 58357 02 A	<input checked="" type="checkbox"/>	Performance monitor	714/39
117	US 58322 92 A	<input checked="" type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
118	US 58298 79 A	<input checked="" type="checkbox"/>	Temperature sensor	374/178
119	US 58290 29 A	<input checked="" type="checkbox"/>	Private cache miss and access management in a multiprocessor system with shared memory	711/133
120	US 58288 60 A	<input checked="" type="checkbox"/>	Data processing device equipped with cache memory and a storage unit for storing data between a main storage or CPU cache memory	712/207
121	US 58260 55 A	<input checked="" type="checkbox"/>	System and method for retiring instructions in a superscalar microprocessor	712/218
122	US 58093 20 A	<input checked="" type="checkbox"/>	High-performance multi-processor having floating point unit	712/34
123	US 58092 68 A	<input checked="" type="checkbox"/>	Method and system for tracking resource allocation within a processor	712/200
124	US 58059 16 A	<input checked="" type="checkbox"/>	Method and apparatus for dynamic allocation of registers for intermediate floating-point results	712/23
125	US 58059 07 A	<input checked="" type="checkbox"/>	System and method for reducing power consumption in an electronic circuit	713/300
126	US 58059 06 A	<input checked="" type="checkbox"/>	Method and apparatus for writing information to registers in a data processing system using a number of registers for processing instructions	710/260
127	US 58058 77 A	<input checked="" type="checkbox"/>	Data processor with branch target address cache and method of operation	712/239
128	US 58054 75 A	<input checked="" type="checkbox"/>	Load-store unit and method of loading and storing single-precision floating-point registers in a double-precision architecture	708/204

	Docum ent ID	U	Title	Current OR
129	US 58025 56 A	<input checked="" type="checkbox"/>	Method and apparatus for correcting misaligned instruction data	711/109
130	US 58022 73 A	<input checked="" type="checkbox"/>	Trailing edge analysis	714/47
131	US 57970 19 A	<input checked="" type="checkbox"/>	Method and system for performance monitoring time lengths of disabled interrupts in a processing system	710/262
132	US 57846 32 A	<input checked="" type="checkbox"/>	Parallel diagonal-fold array processor	712/11
133	US 57846 06 A	<input checked="" type="checkbox"/>	Method and system in a superscalar data processing system for the efficient handling of exceptions	712/244
134	US 57652 08 A	<input checked="" type="checkbox"/>	Method of speculatively executing store instructions prior to performing snoop operations	711/204
135	US 57651 99 A	<input checked="" type="checkbox"/>	Data processor with allocate bit and method of operation	711/168
136	US 57617 23 A	<input checked="" type="checkbox"/>	Data processor with branch prediction and method of operation	711/144
137	US 57548 11 A	<input checked="" type="checkbox"/>	Instruction dispatch queue for improved instruction cache to queue timing	712/214
138	US 57520 62 A	<input checked="" type="checkbox"/>	Method and system for performance monitoring through monitoring an order of processor events during execution in a processing system	714/37
139	US 57519 45 A	<input checked="" type="checkbox"/>	Method and system for performance monitoring stalls to identify pipeline bottlenecks and stalls in a processing system	714/47
140	US 57488 55 A	<input checked="" type="checkbox"/>	Method and system for performance monitoring of misaligned memory accesses in a processing system	712/23
141	US 57457 26 A	<input checked="" type="checkbox"/>	Method and apparatus for selecting the oldest queued instructions without data dependencies	712/216
142	US 57320 05 A	<input checked="" type="checkbox"/>	Single-precision, floating-point register array for floating-point units performing double-precision operations by emulation	708/495
143	US 57297 26 A	<input checked="" type="checkbox"/>	Method and system for performance monitoring efficiency of branch unit operation in a processing system	712/233
144	US 57154 27 A	<input checked="" type="checkbox"/>	Semi-associative cache with MRU/LRU replacement	711/136
145	US 57154 20 A	<input checked="" type="checkbox"/>	Method and system for efficient memory management in a data processing system utilizing a dual mode translation lookaside buffer	711/206
146	US 56995 38 A	<input checked="" type="checkbox"/>	Efficient firm consistency support mechanisms in an out-of-order execution superscalar multiprocessor	712/23
147	US 56919 20 A	<input checked="" type="checkbox"/>	Method and system for performance monitoring of dispatch unit efficiency in a processing system	702/186
148	US 56873 49 A	<input checked="" type="checkbox"/>	Data processor with branch target address cache and subroutine return address cache and method of operation	711/137
149	US 56825 44 A	<input checked="" type="checkbox"/>	Massively parallel diagonal-fold tree array processor	712/16
150	US 56824 95 A	<input checked="" type="checkbox"/>	Fully associative address translation buffer having separate segment and page invalidation	711/207
151	US 56713 82 A	<input checked="" type="checkbox"/>	Information processing system and information processing method for executing instructions in parallel	712/215

	Docum ent ID	U	Title	Current OR
152	US 56689 84 A	<input checked="" type="checkbox"/>	Variable stage load path and method of operation	712/222
153	US 56642 15 A	<input checked="" type="checkbox"/>	Data processor with an execution unit for performing load instructions and method of operation	712/23
154	US 56639 59 A	<input checked="" type="checkbox"/>	ATM cell switching apparatus having a control cell bypass route	370/236 .2
155	US 56550 96 A	<input checked="" type="checkbox"/>	Method and apparatus for dynamic scheduling of instructions to ensure sequentially coherent data in a processor employing out-of-order execution	712/200
156	US 56447 79 A	<input checked="" type="checkbox"/>	Processing system and method of operation for concurrent processing of branch instructions with cancelling of processing of a branch instruction	712/23
157	US 56218 96 A	<input checked="" type="checkbox"/>	Data processor with unified store queue permitting hit under miss memory accesses	711/118
158	US 56130 81 A	<input checked="" type="checkbox"/>	Method of operating a data processor with rapid address comparison for data forwarding	711/3
159	US 56066 82 A	<input checked="" type="checkbox"/>	Data processor with branch target address cache and subroutine return address cache and method of operation	711/204
160	US 56048 79 A	<input checked="" type="checkbox"/>	Single array address translator with segment and page invalidate ability and method of operation	711/207
161	US 55794 93 A	<input checked="" type="checkbox"/>	System with loop buffer and repeat control circuit having stack for storing control information	712/207
162	US 55600 32 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
163	US 55599 76 A	<input checked="" type="checkbox"/>	System for instruction completion independent of result write-back responsive to both exception free completion of execution and completion of all logically prior instructions	712/215
164	US 55532 55 A	<input checked="" type="checkbox"/>	Data processor with programmable levels of speculative instruction fetching and method of operation	712/235
165	US 55509 95 A	<input checked="" type="checkbox"/>	Memory cache with automatic aliased entry invalidation and method of operation	711/3
166	US 55509 74 A	<input checked="" type="checkbox"/>	Testable memory array which is immune to multiple wordline assertions during scan testing	714/42
167	US 55487 38 A	<input checked="" type="checkbox"/>	System and method for processing an instruction in a processing system	712/215
168	US 55465 99 A	<input checked="" type="checkbox"/>	Processing system and method of operation for processing dispatched instructions with detected exceptions	712/23
169	US 55376 02 A	<input checked="" type="checkbox"/>	Process system for controlling bus system to communicate data between resource and processor	712/38
170	US 55354 10 A	<input checked="" type="checkbox"/>	Parallel processor having decoder for selecting switch from the group of switches and concurrently inputting MIMD instructions while performing SIMD operation	712/20
171	US 55353 51 A	<input checked="" type="checkbox"/>	Address translator with by-pass circuit and method of operation	711/207
172	US 55353 46 A	<input checked="" type="checkbox"/>	Data processor with future file with parallel update and method of operation	712/217
173	US 55308 25 A	<input checked="" type="checkbox"/>	Data processor with branch target address cache and method of operation	711/213
174	US 55308 24 A	<input checked="" type="checkbox"/>	Address translation circuit	711/207

	Docum ent ID	U	Title	Current OR
175	US 55308 22 A	<input checked="" type="checkbox"/>	Address translator and method of operation	711/207
176	US 55242 24 A	<input checked="" type="checkbox"/>	System for speculatively executing instructions wherein mispredicted instruction is executed prior to completion of branch processing	712/219
177	US 55111 72 A	<input checked="" type="checkbox"/>	Speculative execution processor	712/235
178	US 55064 37 A	<input checked="" type="checkbox"/>	Microcomputer with high density RAM in separate isolation well on single chip	257/373
179	US 54913 59 A	<input checked="" type="checkbox"/>	Microcomputer with high density ram in separate isolation well on single chip	257/373
180	US 54887 30 A	<input checked="" type="checkbox"/>	Register conflict scoreboard in pipelined computer using pipelined reference counts	712/41
181	US 54816 89 A	<input type="checkbox"/>	Conversion of internal processor register commands to I/O space addresses	711/202
182	US 54715 91 A	<input checked="" type="checkbox"/>	Combined write-operand queue and read-after-write dependency scoreboard	712/217
183	US 54524 67 A	<input checked="" type="checkbox"/>	Microcomputer with high density ram in separate isolation well on single chip	716/1
184	US 54505 55 A	<input checked="" type="checkbox"/>	Register logging in pipelined computer using register log queue of register content changes and base queue of register log queue pointers for respective instructions	712/228
185	US 53945 29 A	<input checked="" type="checkbox"/>	Branch prediction unit for high-performance processor	712/240
186	US 53922 28 A	<input checked="" type="checkbox"/>	Result normalizer and method of operation	708/205
187	US 53865 19 A	<input checked="" type="checkbox"/>	Information processing apparatus incorporating buffer storing a plurality of branch target instructions for branch instructions and interrupt requests	712/238
188	US 53634 95 A	<input checked="" type="checkbox"/>	Data processing system with multiple execution units capable of executing instructions out of sequence	713/500
189	US 53534 26 A	<input checked="" type="checkbox"/>	Cache miss buffer adapted to satisfy read requests to portions of a cache fill in progress without waiting for the cache fill to complete	711/118
190	US 53332 96 A	<input checked="" type="checkbox"/>	Combined queue for invalidates and return data in multiprocessor system	711/171
191	US 53177 20 A	<input checked="" type="checkbox"/>	Processor system with writeback cache using writeback and non writeback transactions stored in separate queues	711/143
192	US 52513 06 A	<input checked="" type="checkbox"/>	Apparatus for controlling execution of a program in a computing device	712/217
193	US 52476 24 A	<input checked="" type="checkbox"/>	Microprogram controller including leading microinstruction from a generator executed while succeeding microinstruction from memory is read out	712/211
194	US 52436 98 A	<input checked="" type="checkbox"/>	Microcomputer	709/201
195	US 52010 57 A	<input checked="" type="checkbox"/>	System for extracting low level concurrency from serial instruction streams	712/18
196	US 51971 37 A	<input checked="" type="checkbox"/>	Computer architecture for the concurrent execution of sequential programs	718/107
197	US 51971 36 A	<input checked="" type="checkbox"/>	Processing system for branch instruction	712/238

	Document ID	U	Title	Current OR
198	US 51858 73 A	<input checked="" type="checkbox"/>	Control system with flag indicating two or less data inputs and counter indicating two or more controlling data driven execution method	712/201
199	US 51858 68 A	<input checked="" type="checkbox"/>	Apparatus having hierarchically arranged decoders concurrently decoding instructions and shifting instructions not ready for execution to vacant decoders higher in the hierarchy	712/217
200	US 51558 43 A	<input checked="" type="checkbox"/>	Error transition mode for multi-processor system	714/5

	L #	Hits	Search Text	DBs
1	L1	12017	(queue buffer fifo) near5 instruction	USPAT; US-PGPUB
2	L3	14667	(issu\$3 dispatch\$3 schedul\$3 execut\$3) near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent\$3 simultaneous\$3))	USPAT; US-PGPUB
3	L6	4226	(queue buffer fifo) near5 instruction	EPO; JPO; DERWENT; IBM_TDB
4	L7	3840	(issu\$3 dispatch\$3 schedul\$3 execut\$3) near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent\$3 simultaneous\$3))	EPO; JPO; DERWENT; IBM_TDB
5	L9	171	6 near99 7	EPO; JPO; DERWENT; IBM_TDB
6	L5	726	1 near99 3	USPAT; US-PGPUB

	Docum ent ID	U	Title	Current OR
1	US 20030 07006 2 A1	<input type="checkbox"/>	System and method for reducing computing system latencies associated with branch instructions	712/234
2	US 20030 07006 0 A1	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
3	US 20030 06590 5 A1	<input type="checkbox"/>	Parallel computation processor, parallel computation control method and program thereof	712/23
4	US 20030 06147 0 A1	<input type="checkbox"/>	Power consumption reduction mechanism for pipeline stalls	712/219
5	US 20030 06146 7 A1	<input type="checkbox"/>	Scoreboarding mechanism in a pipeline that includes replays and redirects	712/217
6	US 20030 06146 5 A1	<input type="checkbox"/>	Issue and retirement mechanism in processor having different pipeline lengths	712/214
7	US 20030 06122 4 A1	<input type="checkbox"/>	Processing system	707/100
8	US 20030 05887 6 A1	<input type="checkbox"/>	Methods and apparatus for retaining packet order in systems utilizing multiple transmit queues	370/412
9	US 20030 05608 9 A1	<input type="checkbox"/>	System and method for handling load and/or store operations in a superscalar microprocessor	712/225
10	US 20030 05608 7 A1	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
11	US 20030 05608 6 A1	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
12	US 20030 04656 3 A1	<input type="checkbox"/>	Encryption-based security protection for processors	713/190
13	US 20030 04385 5 A1	<input type="checkbox"/>	COMMUNICATION NETWORK, AND NODE DEVICE USED THEREIN AND CONTROL METHOD THEREFOR	370/503
14	US 20030 04315 6 A1	<input type="checkbox"/>	Apparatus and method for extracting and loading data to/from a buffer	345/537
15	US 20030 04081 4 A1	<input type="checkbox"/>	Method for controlling mechanisms and technical systems a corresponding device and control software	700/42
16	US 20030 03924 8 A1	<input type="checkbox"/>	System and method for the consolidation of data packets	370/392
17	US 20030 03351 1 A1	<input type="checkbox"/>	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235

	Docum ent ID	U	Title	Current OR
18	US 20030 03351 0 A1	<input type="checkbox"/>	Methods and apparatus for controlling speculative execution of instructions based on a multiaccess memory condition	712/235
19	US 20030 03350 5 A1	<input type="checkbox"/>	Apparatus for processing instructions in a computing system	712/215
20	US 20030 03333 6 A1	<input type="checkbox"/>	Methods for efficient filtering of data	708/300
21	US 20030 02395 9 A1	<input type="checkbox"/>	General and efficient method for transforming predicated execution to static speculation	717/151
22	US 20030 02383 5 A1	<input type="checkbox"/>	Method and system to perform a thread switching operation within a multithreaded processor based on dispatch of a quantity of instruction information for a full instruction	712/214
23	US 20030 02383 4 A1	<input type="checkbox"/>	Method and system to insert a flow marker into an instruction stream to indicate a thread switching operation within a multithreaded processor	712/214
24	US 20030 02365 9 A1	<input type="checkbox"/>	Method and apparatus for thread switching within a multithreaded processor	718/102
25	US 20030 02365 8 A1	<input type="checkbox"/>	Method and system to perform a thread switching operation within a multithreaded processor based on detection of the absence of a flow of instruction information for a thread	718/102
26	US 20030 01868 7 A1	<input type="checkbox"/>	Method and system to perform a thread switching operation within a multithreaded processor based on detection of a flow marker within an instruction information	718/102
27	US 20030 01868 6 A1	<input type="checkbox"/>	Method and system to perform a thread switching operation within a multithreaded processor based on detection of a stall condition	718/102
28	US 20030 01868 5 A1	<input type="checkbox"/>	Method and system to perform a thread switching operation within a multithreaded processor based on detection of a branch instruction	718/102
29	US 20030 00972 7 A1	<input type="checkbox"/>	Circuit designing apparatus, circuit designing method and timing distribution apparatus	716/1
30	US 20030 00962 2 A1	<input type="checkbox"/>	Method and apparatus for resolving additional load misses and page table walks under orthogonal stalls in a single pipeline processor	711/118
31	US 20030 00526 3 A1	<input type="checkbox"/>	Shared resource queue for simultaneous multithreaded processing	712/218
32	US 20020 19445 7 A1	<input type="checkbox"/>	Memory system for ordering load and store instructions in a processor that performs out-of-order multithread execution	712/218
33	US 20020 19445 6 A1	<input type="checkbox"/>	System and method for register renaming	712/217
34	US 20020 18882 9 A1	<input type="checkbox"/>	System and method for handling load and/or store operations in a superscalar microprocessor	712/218

	Docum ent ID	U	Title	Current OR
35	US 20020 18447 9 A1	<input type="checkbox"/>	Bytecode instruction processor with switch instruction handling logic	712/236
36	US 20020 18447 6 A1	<input type="checkbox"/>	Instructions for ordering execution in pipelined processes	712/225
37	US 20020 17834 7 A1	<input type="checkbox"/>	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
38	US 20020 17653 5 A1	<input type="checkbox"/>	Method and system monitoring image detection	378/62
39	US 20020 17438 5 A1	<input type="checkbox"/>	Computer system with debug facility	714/38
40	US 20020 16994 5 A1	<input type="checkbox"/>	Microprocessor	712/205
41	US 20020 16198 7 A1	<input type="checkbox"/>	System and method including distributed instruction buffers holding a second instruction form	712/205
42	US 20020 15699 2 A1	<input type="checkbox"/>	Information processing device and computer system	712/24
43	US 20020 14404 1 A1	<input type="checkbox"/>	Early exception detection	710/260
44	US 20020 13366 1 A1	<input type="checkbox"/>	Data processing system and microcomputer	710/308
45	US 20020 12082 9 A1	<input type="checkbox"/>	Data processor and data processing system	712/207
46	US 20020 12081 3 A1	<input type="checkbox"/>	System and method for multiple store buffer forwarding in a system with a restrictive memory model	711/118
47	US 20020 10802 9 A1	<input type="checkbox"/>	Program counter (PC) relative addressing mode with fast displacement	712/234
48	US 20020 09992 8 A1	<input type="checkbox"/>	Non-stalling circular counterflow pipeline processor with reorder buffer	712/216
49	US 20020 09992 4 A1	<input type="checkbox"/>	Processor	712/24
50	US 20020 09992 2 A1	<input type="checkbox"/>	DATA PROCESSING APPARATUS INCLUDING A PLURALITY OF PIPELINE PROCESSING MECHANISMS IN WHICH MEMORY ACCESS INSTRUCTIONS ARE CARRIED OUT IN A MEMORY ACCESS PIPELINE	712/3
51	US 20020 09991 0 A1	<input type="checkbox"/>	High speed low power cacheless computer system	711/117

	Docum ent ID	U	Title	Current OR
52	US 20020 09566 8 A1	<input type="checkbox"/>	Compiler and register allocation method	717/157
53	US 20020 09566 6 A1	<input type="checkbox"/>	Program optimization method, and compiler using the same	717/149
54	US 20020 09191 4 A1	<input type="checkbox"/>	Multi-threading techniques for a processor utilizing a replay queue	712/219
55	US 20020 08784 9 A1	<input type="checkbox"/>	Full multiprocessor speculation mechanism in a symmetric multiprocessor (smp) System	712/235
56	US 20020 08783 3 A1	<input type="checkbox"/>	Method and apparatus for distributed processor dispersal logic	712/215
57	US 20020 08782 7 A1	<input type="checkbox"/>	Architecture of psm-mpus and coprocessors	712/22
58	US 20020 08339 8 A1	<input type="checkbox"/>	Circuit designing apparatus, circuit designing method and timing distribution apparatus	716/1
59	US 20020 08330 3 A1	<input type="checkbox"/>	Program-controlled unit	712/215
60	US 20020 08330 0 A1	<input type="checkbox"/>	System and method for register renaming	712/203
61	US 20020 07828 5 A1	<input type="checkbox"/>	Reduction of interrupts in remote procedure calls	710/260
62	US 20020 07325 5 A1	<input type="checkbox"/>	Hierarchical selection of direct and indirect counting events in a performance monitor unit	710/104
63	US 20020 06600 5 A1	<input type="checkbox"/>	Data processor with an improved data dependence detector	712/218
64	US 20020 06243 5 A1	<input type="checkbox"/>	PRIORITIZED INSTRUCTION SCHEDULING FOR MULTI-STREAMING PROCESSORS	712/7
65	US 20020 04632 5 A1	<input type="checkbox"/>	Buffer memory management in a system having multiple execution entities	711/122
66	US 20020 03841 5 A1	<input type="checkbox"/>	Processor architecture with independently addressable memory banks for storing instructions to be executed	712/206
67	US 20020 03282 7 A1	<input type="checkbox"/>	STRUCTURE AND METHOD FOR PROVIDING MULTIPLE EXTERNALLY ACCESSIBLE ON-CHIP CACHES IN A MICROPROCESSOR	711/3
68	US 20020 02932 8 A1	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23

	Docum ent ID	U	Title	Current OR
69	US 20020 01690 3 A1	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
70	US 20020 01391 5 A1	<input type="checkbox"/>	Data processing control system, controller, data processing control method, program, and medium	714/6
71	US 20020 00745 0 A1	<input type="checkbox"/>	Line-oriented reorder buffer	712/23
72	US 20010 05414 1 A1	<input type="checkbox"/>	Microsequencer with nested loop counters	712/241
73	US 20010 05414 0 A1	<input type="checkbox"/>	MICROPROCESSOR INCLUDING AN EFFICIENT IMPLEMENTATION OF EXTREME VALUE INSTRUCTIONS	712/223
74	US 20010 05413 8 A1	<input type="checkbox"/>	Instruction buffer and buffer queue control method	712/215
75	US 20010 05413 7 A1	<input type="checkbox"/>	CIRCUIT ARRANGEMENT AND METHOD WITH IMPROVED BRANCH PREFETCHING FOR SHORT BRANCH INSTRUCTIONS	712/11
76	US 20010 05205 5 A1	<input type="checkbox"/>	Active window management for reorder buffer	711/147
77	US 20010 05196 9 A1	<input type="checkbox"/>	Floating point addition pipeline including extreme value, comparison and accumulate functions	708/514
78	US 20010 04977 0 A1	<input type="checkbox"/>	BUFFER MEMORY MANAGEMENT IN A SYSTEM HAVING MULTIPLE EXECUTION ENTITIES	711/129
79	US 20010 04491 2 A1	<input type="checkbox"/>	Reliable hardware support for the use of formal languages in high assurance systems	714/30
80	US 20010 04219 2 A1	<input type="checkbox"/>	Mechanism for self-initiated instruction issuing and method therefor	712/215
81	US 20010 03230 7 A1	<input type="checkbox"/>	MICRO-INSTRUCTION QUEUE FOR A MICROPROCESSOR INSTRUCTION PIPELINE	712/219
82	US 20010 03230 5 A1	<input type="checkbox"/>	Methods and apparatus for dual-use coprocessing/debug interface	712/34
83	US 20010 03094 3 A1	<input type="checkbox"/>	System of controlling the flow of information between senders and receivers across links being used as channels	370/231
84	US 20010 02959 0 A1	<input type="checkbox"/>	Processor having execution core sections operating at different clock rates	713/501
85	US 20010 02531 7 A1	<input type="checkbox"/>	Method of controlling the flow of information between senders and receivers across links being used as channels	709/237

	Docum ent ID	U	Title	Current OR
86	US 20010 02523 7 A1	<input type="checkbox"/>	Computer system with debug facility	703/26
87	US 20010 02342 5 A1	<input type="checkbox"/>	Method and apparatus for rounding in a multiplier arithmetic	708/620
88	US 20010 01873 5 A1	<input type="checkbox"/>	Data processor and data processing system	712/207
89	US 20010 01689 9 A1	<input type="checkbox"/>	Data-processing device	712/215
90	US 20010 01494 1 A1	<input type="checkbox"/>	Processor having multiple program counters and trace buffers outside an execution pipeline	712/228
91	US 20010 01134 3 A1	<input type="checkbox"/>	System and method for register renaming	712/217
92	US 20010 01007 3 A1	<input type="checkbox"/>	Non-stalling circular counterflow pipeline processor with reorder buffer	712/218
93	US 20010 01006 2 A1	<input type="checkbox"/>	Data processing system and microcomputer	710/113
94	US 20010 01005 1 A1	<input type="checkbox"/>	Method and apparatus for multi-function arithmetic	708/502
95	US 65499 85 B1	<input type="checkbox"/>	Method and apparatus for resolving additional load misses and page table walks under orthogonal stalls in a single pipeline processor	711/123
96	US 65430 28 B1	<input type="checkbox"/>	Silent data corruption prevention due to instruction corruption by soft errors	714/800
97	US 65429 86 B1	<input type="checkbox"/>	Resolving dependencies among concurrently dispatched instructions in a superscalar microprocessor	712/217
98	US 65429 84 B1	<input type="checkbox"/>	Scheduler capable of issuing and reissuing dependency chains	712/214
99	US 65429 82 B2	<input type="checkbox"/>	Data processor and data processing system	712/207
100	US 65394 69 B1	<input type="checkbox"/>	Rotator circular buffer with entries to store divided bundles of instructions from each cache line for optimized instruction supply	712/205
101	US 65359 05 B1	<input type="checkbox"/>	Method and apparatus for thread switching within a multithreaded processor	718/108
102	US 65264 21 B1	<input type="checkbox"/>	Method of scheduling garbage collection	707/206
103	US 65231 10 B1	<input type="checkbox"/>	Decoupled fetch-execute engine with static branch prediction support	712/239
104	US 65131 07 B1	<input type="checkbox"/>	Vector transfer system generating address error exception when vector to be transferred does not start and end on same memory page	712/4
105	US 65052 95 B1	<input type="checkbox"/>	Data processor	712/241

	Docum ent ID	U	Title	Current OR
106	US 65048 95 B2	<input type="checkbox"/>	Method and system monitoring image detection	378/19
107	US 64991 00 B1	<input type="checkbox"/>	Enhanced instruction decoding	712/210
108	US 64969 24 B2	<input type="checkbox"/>	Data processing apparatus including a plurality of pipeline processing mechanisms in which memory access instructions are carried out in a memory access pipeline	712/216
109	US 64938 20 B2	<input type="checkbox"/>	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235
110	US 64937 74 B2	<input type="checkbox"/>	Data processing system and microcomputer	710/100
111	US 64906 73 B1	<input type="checkbox"/>	Processor, compiling apparatus, and compile program recorded on a recording medium	712/213
112	US 64876 75 B2	<input type="checkbox"/>	Processor having execution core sections operating at different clock rates	713/501
113	US 64776 39 B1	<input type="checkbox"/>	Branch instruction mechanism for processor	712/237
114	US 64775 99 B1	<input type="checkbox"/>	Data processing system and microcomputer	710/241
115	US 64775 62 B2	<input type="checkbox"/>	Prioritized instruction scheduling for multi-streaming processors	718/108
116	US 64738 50 B1	<input type="checkbox"/>	System and method for handling instructions occurring after an ISYNC instruction	712/244
117	US 64704 22 B2	<input type="checkbox"/>	Buffer memory management in a system having multiple execution entities	711/129
118	US 64635 24 B1	<input type="checkbox"/>	Superscalar processor and method for incrementally issuing store instructions	712/221
119	US 64635 23 B1	<input type="checkbox"/>	Method and apparatus for delaying the execution of dependent loads	712/216
120	US 64635 22 B1	<input type="checkbox"/>	Memory system for ordering load and store instructions in a processor that performs multithread execution	712/216
121	US 64601 30 B1	<input type="checkbox"/>	Detecting full conditions in a queue	712/32
122	US 64601 29 B1	<input type="checkbox"/>	Pipeline operation method and pipeline operation device to interlock the translation of instructions based on the operation of a non-pipeline operation unit	712/31
123	US 64534 12 B1	<input type="checkbox"/>	Method and apparatus for reissuing paired MMX instructions singly during exception handling	712/244
124	US 64534 05 B1	<input type="checkbox"/>	Microprocessor with non-aligned circular addressing	711/201
125	US 64497 10 B1	<input type="checkbox"/>	Stitching parcels	712/216
126	US 64461 97 B1	<input type="checkbox"/>	Two modes for executing branch instructions of different lengths and use of branch control instruction and register set loaded with target instructions	712/237
127	US 64461 64 B1	<input type="checkbox"/>	Test mode accessing of an internal cache memory	711/118
128	US 64426 27 B1	<input type="checkbox"/>	Output FIFO data transfer control device	710/52

	Docum ent ID	U	Title	Current OR
129	US 64426 13 B1	<input type="checkbox"/>	Controlling the flow of information between senders and receivers across links being used as channels	709/232
130	US 64386 73 B1	<input type="checkbox"/>	Correlated address prediction	711/213
131	US 64346 93 B1	<input type="checkbox"/>	System and method for handling load and/or store operations in a superscalar microprocessor	712/245
132	US 64346 91 B1	<input type="checkbox"/>	Cell phones with instruction pre-fetch buffers allocated to low bit address ranges and having validating flags	712/205
133	US 64271 88 B1	<input type="checkbox"/>	Method and system for early tag accesses for lower-level caches in parallel with first-level cache	711/122
134	US 64216 96 B1	<input type="checkbox"/>	System and method for high speed execution of Fast Fourier Transforms utilizing SIMD instructions on a general purpose processor	708/404
135	US 64120 64 B1	<input type="checkbox"/>	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
136	US 64083 75 B2	<input type="checkbox"/>	System and method for register renaming	712/23
137	US 64011 90 B1	<input type="checkbox"/>	Parallel computing units having special registers storing large bit widths	712/24
138	US 63972 39 B2	<input type="checkbox"/>	Floating point addition pipeline including extreme value, comparison and accumulate functions	708/505
139	US 63972 38 B2	<input type="checkbox"/>	Method and apparatus for rounding in a multiplier	708/497
140	US 63935 54 B1	<input type="checkbox"/>	Method and apparatus for performing vector and scalar multiplication and calculating rounded products	712/221
141	US 63935 49 B1	<input type="checkbox"/>	Instruction alignment unit for routing variable byte-length instructions	712/204
142	US 63934 46 B1	<input type="checkbox"/>	32-bit and 64-bit dual mode rotator	708/209
143	US 63895 31 B1	<input type="checkbox"/>	Indexing branch target instruction memory using target address generated by branch control instruction to reduce branch latency	712/237
144	US 63895 12 B1	<input type="checkbox"/>	Microprocessor configured to detect updates to instructions outstanding within an instruction processing pipeline and computer system including same	711/125
145	US 63894 51 B1	<input type="checkbox"/>	Distributed digital rule processor for single system image on a clustered network and method	709/201
146	US 63857 15 B1	<input type="checkbox"/>	Multi-threading for a processor utilizing a replay queue	712/219
147	US 63816 89 B2	<input type="checkbox"/>	Line-oriented reorder buffer configured to selectively store a memory operation result in one of the plurality of reorder buffer storage locations corresponding to the executed instruction	712/215
148	US 63816 25 B2	<input type="checkbox"/>	Method and apparatus for calculating a power of an operand	708/606
149	US 63743 48 B1	<input type="checkbox"/>	Prioritized pre-fetch/preload mechanism for loading and speculative preloading of candidate branch target instruction	712/237
150	US 63670 67 B1	<input type="checkbox"/>	Program conversion apparatus for constant reconstructing VLIW processor	717/154

	Docum ent ID	U	Title	Current OR
151	US 63634 75 B1	<input type="checkbox"/>	Apparatus and method for program level parallelism in a VLIW processor	712/206
152	US 63603 17 B1	<input type="checkbox"/>	Predecoding multiple instructions as one combined instruction and detecting branch to one of the instructions	712/233
153	US 63603 15 B1	<input type="checkbox"/>	Method and apparatus that supports multiple assignment code	712/219
154	US 63603 11 B1	<input type="checkbox"/>	Processor architecture with independently addressable memory banks for storing instructions to be executed	712/206
155	US 63569 97 B1	<input type="checkbox"/>	Emulating branch instruction of different instruction set in a mixed instruction stream in a dual mode system	712/237
156	US 63569 28 B1	<input type="checkbox"/>	Method for partitioning tasks into stateless elements	718/101
157	US 63569 18 B1	<input type="checkbox"/>	Method and system for managing registers in a data processing system supports out-of-order and speculative instruction execution	707/203
158	US 63518 05 B1	<input type="checkbox"/>	Non-stalling circular counterflow pipeline processor with reorder buffer	712/219
159	US 63518 02 B1	<input type="checkbox"/>	Method and apparatus for constructing a pre-scheduled instruction cache	712/215
160	US 63432 88 B1	<input type="checkbox"/>	Single pass space efficient system and method for generating an approximate quantile in a data set having an unknown size	707/7
161	US 63361 54 B1	<input type="checkbox"/>	Method of operating a computer system by identifying source code computational elements in main memory	710/35
162	US 63341 84 B1	<input type="checkbox"/>	Processor and method of fetching an instruction that select one of a plurality of decoded fetch addresses generated in parallel to form a memory request	712/235
163	US 63306 61 B1	<input type="checkbox"/>	Reducing inherited logical to physical register mapping information between tasks in multithread system using register group identifier	712/228
164	US 63306 57 B1	<input type="checkbox"/>	Pairing of micro instructions in the instruction queue	712/23
165	US 63246 43 B1	<input type="checkbox"/>	Branch prediction and target instruction control for processor	712/237
166	US 63246 40 B1	<input type="checkbox"/>	System and method for dispatching groups of instructions using pipelined register renaming	712/217
167	US 63246 39 B1	<input type="checkbox"/>	Instruction converting apparatus using parallel execution code	712/212
168	US 63145 02 B1	<input type="checkbox"/>	Method and apparatus for opportunistic queue processing	711/162
169	US 63112 61 B1	<input type="checkbox"/>	Apparatus and method for improving superscalar processors	712/23
170	US 63082 60 B1	<input type="checkbox"/>	Mechanism for self-initiated instruction issuing and method therefor	712/215
171	US 63082 59 B1	<input type="checkbox"/>	Instruction queue evaluating dependency vector in portions during different clock phases	712/214
172	US 63049 53 B1	<input type="checkbox"/>	Computer processor with instruction-specific schedulers	712/215
173	US 63026 98 B1	<input type="checkbox"/>	Method and apparatus for on-line teaching and learning	434/323

	Docum ent ID	U	Title	Current OR
174	US 62983 67 B1	<input type="checkbox"/>	Floating point addition pipeline including extreme value, comparison and accumulate functions	708/524
175	US 62956 01 B1	<input type="checkbox"/>	System and method using partial trap barrier instruction to provide trap barrier class-based selective stall of instruction processing pipeline	712/244
176	US 62956 00 B1	<input type="checkbox"/>	Thread switch on blocked load or store using instruction thread field	712/228
177	US 62928 45 B1	<input type="checkbox"/>	Processing unit having independent execution units for parallel execution of instructions of different category with instructions having specific bits indicating instruction size and category respectively	710/5
178	US 62894 37 B1	<input type="checkbox"/>	Data processing system and method for implementing an efficient out-of-order issue mechanism	712/217
179	US 62826 30 B1	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
180	US 62791 05 B1	<input type="checkbox"/>	Pipelined two-cycle branch target address cache	712/238
181	US 62791 01 B1	<input type="checkbox"/>	Instruction decoder/dispatch	712/215
182	US 62791 00 B1	<input type="checkbox"/>	Local stall control method and structure in a microprocessor	712/24
183	US 62726 19 B1	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41
184	US 62726 17 B1	<input type="checkbox"/>	System and method for register renaming	712/23
185	US 62694 40 B1	<input type="checkbox"/>	Accelerating vector processing using plural sequencers to process multiple loop iterations simultaneously	712/241
186	US 62693 84 B1	<input type="checkbox"/>	Method and apparatus for rounding and normalizing results within a multiplier	708/497
187	US 62667 61 B1	<input type="checkbox"/>	Method and system in an information processing system for efficient maintenance of copies of values stored within registers	712/23
188	US 62601 38 B1	<input type="checkbox"/>	Method and apparatus for branch instruction processing in a processor	712/239
189	US 62601 35 B1	<input type="checkbox"/>	Parallel processing unit and instruction issuing system	712/214
190	US 62567 45 B1	<input type="checkbox"/>	Processor having execution core sections operating at different clock rates	713/501
191	US 62567 20 B1	<input type="checkbox"/>	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
192	US 62566 53 B1	<input type="checkbox"/>	Multi-function bipartite look-up table	708/290
193	US 62508 21 B1	<input type="checkbox"/>	Method and apparatus for processing branch instructions in an instruction buffer	712/238
194	US 62498 62 B1	<input type="checkbox"/>	Dependency table for reducing dependency checking hardware	712/218
195	US 62471 24 B1	<input type="checkbox"/>	Branch prediction entry with target line index calculated using relative position of second operation of two step branch operation in a line of instructions	712/240

	Docum ent ID	U	Title	Current OR
196	US 62471 21 B1	<input type="checkbox"/>	Multithreading processor with thread predictor	712/239
197	US 62471 20 B1	<input type="checkbox"/>	Instruction buffer for issuing instruction sets to an instruction decoder	712/238
198	US 62471 15 B1	<input type="checkbox"/>	Non-stalling circular counterflow pipeline processor with reorder buffer	712/219
199	US 62471 14 B1	<input type="checkbox"/>	Rapid selection of oldest eligible entry in a queue	712/216
200	US 62470 64 B1	<input type="checkbox"/>	Enqueue instruction in a system architecture for improved message passing and process synchronization	719/312

	L #	Hits	Search Text	DBs
1	L1	12017	(queue buffer fifo) near5 instruction	USPAT; US-PGPUB
2	L3	13601	execut\$3 near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent\$3 simultaneous\$3))	USPAT; US-PGPUB
3	L5	1850	1 near30 ((select\$3 multiplex\$3 rout\$3 switch\$3 crossbar) near10 instruction)	USPAT; US-PGPUB
4	L6	65	5 near99 3	USPAT; US-PGPUB
5	L7	4226	(queue buffer fifo) near5 instruction	EPO; JPO; DERWENT; IBM_TDB
6	L8	398	7 near30 ((select\$3 multiplex\$3 rout\$3 switch\$3 crossbar) near10 instruction)	EPO; JPO; DERWENT; IBM_TDB
7	L9	3446	execut\$3 near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent\$3 simultaneous\$3))	EPO; JPO; DERWENT; IBM_TDB
8	L10	37	8 and 9	EPO; JPO; DERWENT; IBM_TDB
9	L18	225	5 near20 ((process\$3 function\$3 execut\$3) adj2 (unit element module)) not 6	USPAT; US-PGPUB
10	L19	830	3 and 5 not (6 18)	USPAT; US-PGPUB
11	L20	220	((queue buffer fifo) near5 instruction).ab,ti. and 19	USPAT; US-PGPUB

	Docum ent ID	U	Title	Current OR
1	US 20040 03995 2 A1	<input type="checkbox"/>	Method and apparatus for power reduction in a digital signal processor integrated circuit	713/300
2	US 20040 03086 6 A1	<input type="checkbox"/>	Apparatus and method for buffering instructions and late-generated related information using history of previous load/shifts	712/217
3	US 20040 03086 5 A1	<input type="checkbox"/>	Method and apparatus for implementing two architectures in a chip	712/209
4	US 20040 00320 3 A1	<input type="checkbox"/>	Instruction fetch control device and instruction fetch control method	712/205
5	US 20040 00320 2 A1	<input type="checkbox"/>	Instruction fetch control apparatus	712/205
6	US 20030 21272 6 A1	<input type="checkbox"/>	Floating point unit power reduction scheme	708/501
7	US 20030 16367 9 A1	<input type="checkbox"/>	Method and apparatus for loop buffering digital signal processing instructions	712/241
8	US 20030 15435 8 A1	<input type="checkbox"/>	Apparatus and method for dispatching very long instruction word having variable length	712/24
9	US 20030 13571 9 A1	<input type="checkbox"/>	Method and system using hardware assistance for tracing instruction disposition information	712/227
10	US 20030 13571 8 A1	<input type="checkbox"/>	Method and system using hardware assistance for instruction tracing by revealing executed opcode or instruction	712/227
11	US 20030 12089 8 A1	<input type="checkbox"/>	Method and circuits for early detection of a full queue	712/205
12	US 20030 08427 3 A1	<input type="checkbox"/>	Processor and method of testing a processor for hardware faults utilizing a pipeline interlocking test instruction	712/227
13	US 20030 06146 6 A1	<input type="checkbox"/>	Method and apparatus for fast dependency coordinate matching	712/217
14	US 20030 05613 4 A1	<input type="checkbox"/>	Method and apparatus for power reduction in a digital signal processor integrated circuit	713/324
15	US 20030 00962 2 A1	<input type="checkbox"/>	Method and apparatus for resolving additional load misses and page table walks under orthogonal stalls in a single pipeline processor	711/118
16	US 20030 00526 2 A1	<input type="checkbox"/>	Mechanism for providing high instruction fetch bandwidth in a multi-threaded processor	712/207
17	US 20030 00468 3 A1	<input type="checkbox"/>	Instruction pre-fetching mechanism for a multithreaded program execution	702/186

	Docum ent ID	U	Title	Current OR
18	US 20020 16198 7 A1	<input type="checkbox"/>	System and method including distributed instruction buffers holding a second instruction form	712/205
19	US 20020 12082 9 A1	<input type="checkbox"/>	Data processor and data processing system	712/207
20	US 20020 10397 1 A1	<input type="checkbox"/>	Control circuit for cache system and method of controlling cache system	711/118
21	US 20020 09191 4 A1	<input type="checkbox"/>	Multi-threading techniques for a processor utilizing a replay queue	712/219
22	US 20020 08783 2 A1	<input type="checkbox"/>	Instruction fetch apparatus for wide issue processors and method of operation	712/206
23	US 20020 08330 2 A1	<input type="checkbox"/>	Hardware instruction translation within a processor pipeline	712/209
24	US 20020 00745 0 A1	<input type="checkbox"/>	Line-oriented reorder buffer	712/23
25	US 20010 03744 4 A1	<input type="checkbox"/>	INSTRUCTION BUFFERING MECHANISM	712/207
26	US 20010 01873 5 A1	<input type="checkbox"/>	Data processor and data processing system	712/207
27	US 20010 01689 9 A1	<input type="checkbox"/>	Data-processing device	712/215
28	US 67048 56 B1	<input type="checkbox"/>	Method for compacting an instruction queue	712/215
29	US 67014 26 B1	<input type="checkbox"/>	Switching between a plurality of branch prediction processes based on which instruction set is operational wherein branch history data structures are the same for the plurality of instruction sets	712/239
30	US 66912 21 B2	<input type="checkbox"/>	Loading previously dispatched slots in multiple instruction dispatch buffer before dispatching remaining slots for parallel execution	712/215
31	US 66878 57 B1	<input type="checkbox"/>	Microcomputer which can execute a monitor program supplied from a debugging tool	714/38
32	US 66622 97 B1	<input type="checkbox"/>	Allocation of processor bandwidth by inserting interrupt servicing instructions to intervene main program in instruction queue mechanism	712/245
33	US 66368 83 B1	<input type="checkbox"/>	Mechanism for passing information between queuing and de-queuing processes	718/102
34	US 66188 01 B1	<input type="checkbox"/>	Method and apparatus for implementing two architectures in a chip using bundles that contain microinstructions and template information	712/215
35	US 66092 01 B1	<input type="checkbox"/>	Secure program execution using instruction buffer interdependencies	713/187
36	US 66091 91 B1	<input type="checkbox"/>	Method and apparatus for speculative microinstruction pairing	712/216

	Docum ent ID	U	Title	Current OR
37	US 66041 91 B1	<input type="checkbox"/>	Method and apparatus for accelerating instruction fetching for a processor	712/207
38	US 65981 55 B1	<input type="checkbox"/>	Method and apparatus for loop buffering digital signal processing instructions	712/241
39	US 65713 29 B1	<input type="checkbox"/>	Detection of overwrite modification by preceding instruction possibility of fetched instruction code using fetched instructions counter and store target address	712/205
40	US 65534 84 B1	<input type="checkbox"/>	Instruction-issuing circuit that sets reference dependency information in a preceding instruction when a succeeding instruction is stored in an instruction out-of-order buffer	712/217
41	US 65534 82 B1	<input type="checkbox"/>	Universal dependency vector/queue entry	712/216
42	US 65500 03 B1	<input type="checkbox"/>	Not reported jump buffer	712/218
43	US 65499 85 B1	<input type="checkbox"/>	Method and apparatus for resolving additional load misses and page table walks under orthogonal stalls in a single pipeline processor	711/123
44	US 65429 87 B1	<input type="checkbox"/>	Method and circuits for early detection of a full queue	712/217
45	US 65429 82 B2	<input type="checkbox"/>	Data processor and data processing system	712/207
46	US 65394 69 B1	<input type="checkbox"/>	Rotator circular buffer with entries to store divided bundles of instructions from each cache line for optimized instruction supply	712/205
47	US 65300 13 B1	<input type="checkbox"/>	Instruction control apparatus for loading plurality of instructions into execution stage	712/206
48	US 64776 40 B1	<input type="checkbox"/>	Apparatus and method for predicting multiple branches and performing out-of-order branch resolution	712/238
49	US 64704 43 B1	<input type="checkbox"/>	Pipelined multi-thread processor selecting thread instruction in inter-stage buffer based on count information	712/205
50	US 64635 24 B1	<input type="checkbox"/>	Superscalar processor and method for incrementally issuing store instructions	712/221
51	US 64601 30 B1	<input type="checkbox"/>	Detecting full conditions in a queue	712/32
52	US 64427 07 B1	<input type="checkbox"/>	Alternate fault handler	714/10
53	US 64426 81 B1	<input type="checkbox"/>	Pipelined central processor managing the execution of instructions with proximate successive branches in a cache-based data processing system while performing block mode transfer predictions	712/238
54	US 64346 91 B1	<input type="checkbox"/>	Cell phones with instruction pre-fetch buffers allocated to low bit address ranges and having validating flags	712/205
55	US 63935 36 B1	<input type="checkbox"/>	Load/store unit employing last-in-buffer indication for rapid load-hit-store	711/159
56	US 63895 31 B1	<input type="checkbox"/>	Indexing branch target instruction memory using target address generated by branch control instruction to reduce branch latency	712/237
57	US 63857 15 B1	<input type="checkbox"/>	Multi-threading for a processor utilizing a replay queue	712/219
58	US 63816 89 B2	<input type="checkbox"/>	Line-oriented reorder buffer configured to selectively store a memory operation result in one of the plurality of reorder buffer storage locations corresponding to the executed instruction	712/215

	Docum ent ID	U	Title	Current OR
59	US 63743 48 B1	<input type="checkbox"/>	Prioritized pre-fetch/preload mechanism for loading and speculative preloading of candidate branch target instruction	712/237
60	US 63670 06 B1	<input type="checkbox"/>	Predecode buffer including buffer pointer indicating another buffer for predecoding	712/244
61	US 63518 02 B1	<input type="checkbox"/>	Method and apparatus for constructing a pre-scheduled instruction cache	712/215
62	US 63413 47 B1	<input type="checkbox"/>	Thread switch logic in a multiple-thread processor	712/228
63	US 63381 33 B1	<input type="checkbox"/>	Measured, allocation of speculative branch instructions to processor execution units	712/214
64	US 63213 25 B1	<input type="checkbox"/>	Dual in-line buffers for an instruction fetch unit	712/204
65	US 63213 10 B1	<input type="checkbox"/>	Memory architecture for a computer system	711/154
66	US 63145 09 B1	<input type="checkbox"/>	Efficient method for fetching instructions having a non-power of two size	712/204
67	US 63112 61 B1	<input type="checkbox"/>	Apparatus and method for improving superscalar processors	712/23
68	US 63082 59 B1	<input type="checkbox"/>	Instruction queue evaluating dependency vector in portions during different clock phases	712/214
69	US 62928 84 B1	<input type="checkbox"/>	Reorder buffer employing last in line indication	712/216
70	US 62928 82 B1	<input type="checkbox"/>	Method and apparatus for filtering valid information for downstream processing	712/204
71	US 62928 45 B1	<input type="checkbox"/>	Processing unit having independent execution units for parallel execution of instructions of different category with instructions having specific bits indicating instruction size and category respectively	710/5
72	US 62894 37 B1	<input type="checkbox"/>	Data processing system and method for implementing an efficient out-of-order issue mechanism	712/217
73	US 62726 20 B1	<input type="checkbox"/>	Central processing unit having instruction queue of 32-bit length fetching two instructions of 16-bit fixed length in one instruction fetch operation	712/41
74	US 62533 05 B1	<input type="checkbox"/>	Microprocessor for supporting reduction of program codes in size	712/32
75	US 62498 62 B1	<input type="checkbox"/>	Dependency table for reducing dependency checking hardware	712/218
76	US 62471 14 B1	<input type="checkbox"/>	Rapid selection of oldest eligible entry in a queue	712/216
77	US 62405 08 B1	<input type="checkbox"/>	Decode and execution synchronized pipeline processing using decode generated memory read queue with stop entry to allow execution generated memory read	712/219
78	US 62405 07 B1	<input type="checkbox"/>	Mechanism for multiple register renaming and method therefor	712/217
79	US 62370 82 B1	<input type="checkbox"/>	Reorder buffer configured to allocate storage for instruction results corresponding to predefined maximum number of concurrently receivable instructions independent of a number of instructions received	712/215
80	US 62370 79 B1	<input type="checkbox"/>	Coprocessor interface having pending instructions queue and clean-up queue and dynamically allocating memory	712/34

	Docum ent ID	U	Title	Current OR
81	US 62162 00 B1	<input type="checkbox"/>	Address queue	711/100
82	US 62126 23 B1	<input type="checkbox"/>	Universal dependency vector/queue entry	712/216
83	US 62090 84 B1	<input type="checkbox"/>	Dependency table for reducing dependency checking hardware	712/233
84	US 61924 65 B1	<input type="checkbox"/>	Using multiple decoders and a reorder queue to decode instructions out of order	712/212
85	US 61924 61 B1	<input type="checkbox"/>	Method and apparatus for facilitating multiple storage instruction completions in a superscalar processor during a single clock cycle	712/23
86	US 61890 92 B1	<input type="checkbox"/>	Pipeline processor capable of reducing branch hazards with small-scale circuit	712/241
87	US 61890 89 B1	<input type="checkbox"/>	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/218
88	US 61890 87 B1	<input type="checkbox"/>	Superscalar instruction decoder including an instruction queue	712/208
89	US 61856 72 B1	<input type="checkbox"/>	Method and apparatus for instruction queue compression	712/217
90	US 61784 97 B1	<input type="checkbox"/>	System and method for determining the relative age of instructions in a processor	712/214
91	US 61758 97 B1	<input type="checkbox"/>	Synchronization of branch cache searches and allocation/modification/deletion of branch cache	711/119
92	US 61579 98 A	<input type="checkbox"/>	Method for performing branch prediction and resolution of two or more branch instructions within two or more branch prediction buffers	712/238
93	US 61426 83 A	<input type="checkbox"/>	Debug interface including data steering between a processor, an input/output port, and a trace logic	717/128
94	US 61417 42 A	<input type="checkbox"/>	Method for reducing number of bits used in storage of instruction address pointer values	711/220
95	US 61346 51 A	<input type="checkbox"/>	Reorder buffer employed in a microprocessor to store instruction results having a plurality of entries predetermined to correspond to a plurality of functional units	712/215
96	US 61287 22 A	<input type="checkbox"/>	Data processing system having an apparatus for exception tracking during out-of-order operation and method therefor	712/23
97	US 61227 29 A	<input type="checkbox"/>	Prefetch buffer which stores a pointer indicating an initial predecode position	712/244
98	US 61227 27 A	<input type="checkbox"/>	Symmetrical instructions queue for high clock frequency scheduling	712/214
99	US 61227 24 A	<input type="checkbox"/>	Central processing unit having instruction queue of 32-bit length fetching two instructions of 16-bit fixed length in one instruction fetch operation	712/41
100	US 61192 20 A	<input type="checkbox"/>	Method of and apparatus for supplying multiple instruction strings whose addresses are discontinued by branch instructions	712/235
101	US 61158 07 A	<input type="checkbox"/>	Static instruction decoder utilizing a circular queue to decode instructions and select instructions to be issued	712/212
102	US 61120 19 A	<input type="checkbox"/>	Distributed instruction queue	712/214

	Docum ent ID	U	Title	Current OR
103	US 61087 75 A	<input type="checkbox"/>	Dynamically loadable pattern history tables in a multi-task microprocessor	712/240
104	US 61087 69 A	<input type="checkbox"/>	Dependency table for reducing dependency checking hardware	712/216
105	US 60853 11 A	<input type="checkbox"/>	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/204
106	US 60852 97 A	<input type="checkbox"/>	Single-chip memory system including buffer	711/158
107	US 60731 59 A	<input type="checkbox"/>	Thread properties attribute vector based thread selection in multithreading processor	718/103
108	US 60651 12 A	<input type="checkbox"/>	Microprocessor with arithmetic processing units and arithmetic execution unit	712/221
109	US 60651 10 A	<input type="checkbox"/>	Method and apparatus for loading an instruction buffer of a processor capable of out-of-order instruction issue	712/217
110	US 60527 08 A	<input type="checkbox"/>	Performance monitoring of thread switch events in a multithreaded processor	718/108
111	US 60322 51 A	<input type="checkbox"/>	Computer system including a microprocessor having a reorder buffer employing last in buffer and last in line indications	712/216
112	US 60264 82 A	<input type="checkbox"/>	Recorder buffer and a method for allocating a fixed amount of storage for instruction results independent of a number of concurrently dispatched instructions	712/215
113	US 60214 88 A	<input type="checkbox"/>	Data processing system having an apparatus for tracking a status of an out-of-order operation and method thereof	712/228
114	US 59960 71 A	<input type="checkbox"/>	Detecting self-modifying code in a pipelined processor with branch processing by comparing latched store address to subsequent target address	712/238
115	US 59833 42 A	<input type="checkbox"/>	Superscalar microprocessor employing a future file for storing results into multiportion registers	712/218
116	US 59742 40 A	<input type="checkbox"/>	Method and system for buffering condition code data in a data processing system having out-of-order and speculative instruction execution	712/218
117	US 59616 34 A	<input type="checkbox"/>	Reorder buffer having a future file for storing speculative instruction execution results	712/218
118	US 59604 67 A	<input type="checkbox"/>	Apparatus for efficiently providing memory operands for instructions	711/214
119	US 59580 43 A	<input type="checkbox"/>	Superscalar processor with forward map buffer in multiple instruction parallel issue/execution management system	712/216
120	US 59516 75 A	<input type="checkbox"/>	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/215
121	US 59464 68 A	<input type="checkbox"/>	Reorder buffer having an improved future file for storing speculative instruction execution results	712/218
122	US 59448 11 A	<input type="checkbox"/>	Superscalar processor with parallel issue and execution device having forward map of operand and instruction dependencies	712/23
123	US 59352 41 A	<input type="checkbox"/>	Multiple global pattern history tables for branch prediction in a microprocessor	712/240
124	US 59305 20 A	<input type="checkbox"/>	Pipelining device in a parallel processing apparatus and an instruction supplying method therefor	712/23
125	US 59238 62 A	<input type="checkbox"/>	Processor that decodes a multi-cycle instruction into single-cycle micro-instructions and schedules execution of the micro-instructions	712/208

	Docum ent ID	U	Title	Current OR
126	US 59151 10 A	<input type="checkbox"/>	Branch misprediction recovery in a reorder buffer having a future file	712/239
127	US 59130 59 A	<input type="checkbox"/>	Multi-processor system for inheriting contents of register from parent thread to child thread	718/104
128	US 59037 40 A	<input type="checkbox"/>	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/217
129	US 58965 18 A	<input type="checkbox"/>	Instruction queue scanning using opcode identification	712/208
130	US 58871 85 A	<input type="checkbox"/>	Interface for coupling a floating point unit to a reorder buffer	712/23
131	US 58871 61 A	<input type="checkbox"/>	Issuing instructions in a processor supporting out-of-order execution	712/244
132	US 58871 52 A	<input type="checkbox"/>	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
133	US 58729 51 A	<input type="checkbox"/>	Reorder buffer having a future file for storing speculative instruction execution results	712/218
134	US 58729 46 A	<input type="checkbox"/>	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/204
135	US 58676 98 A	<input type="checkbox"/>	Apparatus and method for accessing a branch target buffer	712/238
136	US 58646 90 A	<input type="checkbox"/>	Apparatus and method for register specific fill-in of register generic micro instructions within an instruction queue	712/208
137	US 58599 92 A	<input type="checkbox"/>	Instruction alignment using a dispatch list and a latch list	712/204
138	US 58505 42 A	<input type="checkbox"/>	Microprocessor instruction hedge-fetching in a multiprediction branch environment	712/235
139	US 58482 69 A	<input type="checkbox"/>	Branch predicting mechanism for enhancing accuracy in branch prediction by reference to data	712/239
140	US 58451 01 A	<input type="checkbox"/>	Prefetch buffer for storing instructions prior to placing the instructions in an instruction cache	712/207
141	US 58451 00 A	<input type="checkbox"/>	Dual instruction buffers with a bypass bus and rotator for a decoder of multiple instructions of variable length	712/204
142	US 58359 68 A	<input type="checkbox"/>	Apparatus for providing memory and register operands concurrently to functional units	711/214
143	US 58290 21 A	<input type="checkbox"/>	System for controlling operating timing of a cache memory	711/118
144	US 58260 96 A	<input type="checkbox"/>	Minimal instruction set computer architecture and multiple instruction issue method	712/24
145	US 58225 74 A	<input type="checkbox"/>	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
146	US 58225 55 A	<input type="checkbox"/>	Method and apparatus for aligning an instruction boundary in variable length macroinstructions with an instruction buffer	712/204
147	US 58190 56 A	<input type="checkbox"/>	Instruction buffer organization method and system	712/204
148	US 58058 78 A	<input type="checkbox"/>	Method and apparatus for generating branch predictions for multiple branch instructions indexed by a single instruction pointer	712/239

	Docum ent ID	U	Title	Current OR
149	US 58058 53 A	<input type="checkbox"/>	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
150	US 58058 52 A	<input type="checkbox"/>	Parallel processor performing bypass control by grasping portions in which instructions exist	712/218
151	US 57969 98 A	<input type="checkbox"/>	Apparatus and method for performing branch target address calculation and branch prediciton in parallel in an information handling system	712/239
152	US 57782 46 A	<input type="checkbox"/>	Method and apparatus for efficient propagation of attribute bits in an instruction decode pipeline	712/23
153	US 57685 55 A	<input type="checkbox"/>	Reorder buffer employing last in buffer and last in line bits	712/216
154	US 57652 20 A	<input type="checkbox"/>	Apparatus and method to reduce instruction address storage in a super-scaler processor	711/220
155	US 57649 70 A	<input type="checkbox"/>	Method and apparatus for supporting speculative branch and link/branch on count instructions	712/233
156	US 57649 38 A	<input type="checkbox"/>	Resynchronization of a superscalar processor	712/200
157	US 57548 13 A	<input type="checkbox"/>	Data processor	712/216
158	US 57489 78 A	<input type="checkbox"/>	Byte queue divided into multiple subqueues for optimizing instruction selection logic	712/23
159	US 57427 81 A	<input type="checkbox"/>	Decoded instruction buffer apparatus and method for reducing power consumption in a digital signal processor	712/208
160	US 57218 57 A	<input type="checkbox"/>	Method and apparatus for saving the effective address of floating point memory operations in an out-of-order microprocessor	712/23
161	US 57064 92 A	<input type="checkbox"/>	Method and apparatus for implementing a set-associative branch target buffer	712/238
162	US 56995 37 A	<input type="checkbox"/>	Processor microarchitecture for efficient dynamic scheduling and execution of chains of dependent instructions	712/217
163	US 56805 97 A	<input type="checkbox"/>	System with flexible local control for modifying same instruction partially in different processor of a SIMD computer system to execute dissimilar sequences of instructions	712/226
164	US 56805 65 A	<input type="checkbox"/>	Method and apparatus for performing page table walks in a microprocessor capable of processing speculative instructions	711/205
165	US 56492 25 A	<input type="checkbox"/>	Resynchronization of a superscalar processor	712/23
166	US 56320 23 A	<input type="checkbox"/>	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
167	US 56300 82 A	<input type="checkbox"/>	Apparatus and method for instruction queue scanning	712/213
168	US 56236 15 A	<input type="checkbox"/>	Circuit and method for reducing prefetch cycles on microprocessors	712/238
169	US 56197 30 A	<input type="checkbox"/>	Pipelining device in a parallel processing apparatus and an instruction supplying method therefor	710/35
170	US 56196 67 A	<input type="checkbox"/>	Method and apparatus for fast fill of translator instruction queue	712/208

	Docum ent ID	U	Title	Current OR
171	US 56196 63 A	<input type="checkbox"/>	Computer instruction prefetch system	712/207
172	US 56088 85 A	<input type="checkbox"/>	Method for handling instructions from a branch prior to instruction decoding in a computer which executes variable-length instructions	712/204
173	US 56029 98 A	<input type="checkbox"/>	Dequeue instruction in a system architecture for improved message passing and process synchronization	712/225
174	US 56008 06 A	<input type="checkbox"/>	Method and apparatus for aligning an instruction boundary in variable length macroinstructions with an instruction buffer	712/204
175	US 55985 44 A	<input type="checkbox"/>	Instruction buffer device for processing an instruction set of variable-length instruction codes	712/204
176	US 55862 77 A	<input type="checkbox"/>	Method for parallel steering of fixed length fields containing a variable length instruction from an instruction buffer to parallel decoders	712/210
177	US 55748 71 A	<input type="checkbox"/>	Method and apparatus for implementing a set-associative branch target buffer	712/200
178	US 55640 41 A	<input type="checkbox"/>	Microprocessor for inserting a bus cycle in an instruction set to output an internal information for an emulation	703/23
179	US 55532 54 A	<input type="checkbox"/>	Instruction cache access and prefetch process controlled by a predicted instruction-path mechanism	712/207
180	US 55420 58 A	<input type="checkbox"/>	Pipelined computer with operand context queue to simplify context-dependent execution flow	713/502
181	US 55375 59 A	<input type="checkbox"/>	Exception handling circuit and method	712/244
182	US 55091 30 A	<input type="checkbox"/>	Method and apparatus for grouping multiple instructions, issuing grouped instructions simultaneously, and executing grouped instructions in a pipelined processor	712/215
183	US 55009 48 A	<input type="checkbox"/>	Translating instruction pointer virtual addresses to physical addresses for accessing an instruction cache	711/205
184	US 54817 43 A	<input type="checkbox"/>	Minimal instruction set computer architecture and multiple instruction issue method	712/23
185	US 54674 73 A	<input type="checkbox"/>	Out of order instruction load and store comparison	712/23
186	US 54487 05 A	<input type="checkbox"/>	RISC microprocessor architecture implementing fast trap and exception state	712/244
187	US 54230 16 A	<input type="checkbox"/>	Block buffer for instruction/operand caches	711/123
188	US 53718 64 A	<input type="checkbox"/>	Apparatus for concurrent multiple instruction decode in variable length instruction set computer	712/206
189	US 53177 01 A	<input type="checkbox"/>	Method for refilling instruction queue by reading predetermined number of instruction words comprising one or more instructions and determining the actual number of instruction words used	712/207
190	US 52652 13 A	<input type="checkbox"/>	Pipeline system for executing predicted branch target instruction in a cycle concurrently with the execution of branch instruction	712/240
191	US 52631 69 A	<input type="checkbox"/>	Bus arbitration and resource management for concurrent vector signal processor architecture	712/7
192	US 51971 45 A	<input type="checkbox"/>	Buffer storage system using parallel buffer storage units and move-out buffer registers	711/143

	Docum ent ID	U	Title	Current OR
193	US 51971 31 A	<input type="checkbox"/>	Instruction buffer system for switching execution of current instruction to a branch or to a return from subroutine	712/238
194	US 51704 74 A	<input type="checkbox"/>	Method of searching a queue in response to a search instruction	707/6
195	US 51485 28 A	<input type="checkbox"/>	Method and apparatus for simultaneously decoding three operands in a variable length instruction when one of the operands is also of variable length	712/210
196	US 51426 33 A	<input type="checkbox"/>	Preprocessing implied specifiers in a pipelined processor	712/225
197	US 51194 95 A	<input type="checkbox"/>	Minimizing hardware pipeline breaks using software scheduling techniques during compilation	717/153
198	US 51135 15 A	<input type="checkbox"/>	Virtual instruction cache system using length responsive decoded instruction shifting and merging with prefetch buffer outputs to fill instruction buffer	711/125
199	US 51013 41 A	<input type="checkbox"/>	Pipelined system for reducing instruction access time by accumulating predecoded instruction bits a FIFO	712/213
200	US 50816 98 A	<input type="checkbox"/>	Method and apparatus for graphics display data manipulation	345/422

	L #	Hits	Search Text	DBs
1	L1	12017	(queue buffer fifo) near5 instruction	USPAT; US-PGPUB
2	L3	14667	(issu\$3 dispatch\$3 schedul\$3 execut\$3) near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent\$3 simultaneous\$3))	USPAT; US-PGPUB
3	L6	4226	(queue buffer fifo) near5 instruction	EPO; JPO; DERWENT; IBM_TDB
4	L7	3840	(issu\$3 dispatch\$3 schedul\$3 execut\$3) near10 (instruction near10 (multiple multiplicity plural plurality parallel concurrent\$3 simultaneous\$3))	EPO; JPO; DERWENT; IBM_TDB
5	L9	171	6 near99 7	EPO; JPO; DERWENT; IBM_TDB
6	L5	726	1 near99 3	USPAT; US-PGPUB

	Docum ent ID	U	Title	Current OR
1	US 62471 24 B1	<input type="checkbox"/>	Branch prediction entry with target line index calculated using relative position of second operation of two step branch operation in a line of instructions	712/240
2	US 62471 21 B1	<input type="checkbox"/>	Multithreading processor with thread predictor	712/239
3	US 62471 20 B1	<input type="checkbox"/>	Instruction buffer for issuing instruction sets to an instruction decoder	712/238
4	US 62471 15 B1	<input type="checkbox"/>	Non-stalling circular counterflow pipeline processor with reorder buffer	712/219
5	US 62471 14 B1	<input type="checkbox"/>	Rapid selection of oldest eligible entry in a queue	712/216
6	US 62470 64 B1	<input type="checkbox"/>	Enqueue instruction in a system architecture for improved message passing and process synchronization	719/312
7	US 62438 36 B1	<input type="checkbox"/>	Apparatus and method for circular buffering on an on-chip discontinuity trace	714/45
8	US 62405 09 B1	<input type="checkbox"/>	Out-of-pipeline trace buffer for holding instructions that may be re-executed following misspeculation	712/228
9	US 62405 08 B1	<input type="checkbox"/>	Decode and execution synchronized pipeline processing using decode generated memory read queue with stop entry to allow execution generated memory read	712/219
10	US 62370 83 B1	<input type="checkbox"/>	Microprocessor including multiple register files mapped to the same logical storage and inhibiting sychronization between the register files responsive to inclusion of an instruction in an instruction sequence	712/217
11	US 62370 82 B1	<input type="checkbox"/>	Reorder buffer configured to allocate storage for instruction results corresponding to predefined maximum number of concurrently receivable instructions independent of a number of instructions received	712/215
12	US 62302 54 B1	<input type="checkbox"/>	System and method for handling load and/or store operators in a superscalar microprocessor	712/23
13	US 62266 41 B1	<input type="checkbox"/>	Access control for groups of related data items	707/8
14	US 62231 98 B1	<input type="checkbox"/>	Method and apparatus for multi-function arithmetic	708/620
15	US 62231 92 B1	<input type="checkbox"/>	Bipartite look-up table with output values having minimized absolute error	708/270
16	US 62162 34 B1	<input type="checkbox"/>	Processor having execution core sections operating at different clock rates	713/501
17	US 62090 84 B1	<input type="checkbox"/>	Dependency table for reducing dependency checking hardware	712/233
18	US 62090 82 B1	<input type="checkbox"/>	Apparatus and method for optimizing execution of push all/pop all instructions	712/225
19	US 62090 81 B1	<input type="checkbox"/>	Method and system for nonsequential instruction dispatch and execution in a superscalar processor system	712/215
20	US 62055 42 B1	<input type="checkbox"/>	Processor pipeline including replay	712/219
21	US 61924 68 B1	<input type="checkbox"/>	Apparatus and method for detecting microbranches early	712/231
22	US 61924 66 B1	<input type="checkbox"/>	Pipeline control for high-frequency pipelined designs	712/214

	Docum ent ID	U	Title	Current OR
23	US 61924 61 B1	<input type="checkbox"/>	Method and apparatus for facilitating multiple storage instruction completions in a superscalar processor during a single clock cycle	712/23
24	US 61890 89 B1	<input type="checkbox"/>	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/218
25	US 61856 72 B1	<input type="checkbox"/>	Method and apparatus for instruction queue compression	712/217
26	US 61822 10 B1	<input type="checkbox"/>	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235
27	US 61759 10 B1	<input type="checkbox"/>	Speculative instructions execution in VLIW processors	712/217
28	US 61700 51 B1	<input type="checkbox"/>	Apparatus and method for program level parallelism in a VLIW processor	712/225
29	US 61675 07 A	<input type="checkbox"/>	Apparatus and method for floating point exchange dispatch with reduced latency	712/213
30	US 61675 03 A	<input type="checkbox"/>	Register and instruction controller for superscalar processor	712/23
31	US 61638 39 A	<input type="checkbox"/>	Non-stalling circular counterflow pipeline processor with reorder buffer	712/219
32	US 61638 21 A	<input type="checkbox"/>	Method and apparatus for balancing load vs. store access to a primary data cache	710/57
33	US 61611 72 A	<input type="checkbox"/>	Method for concurrently dispatching microcode and directly-decoded instructions in a microprocessor	712/204
34	US 61579 88 A	<input type="checkbox"/>	Method and apparatus for high performance branching in pipelined microsystems	711/140
35	US 61547 65 A	<input type="checkbox"/>	Distributed digital rule processor for single system image on a clustered network and method	709/201
36	US 61483 95 A	<input type="checkbox"/>	Shared floating-point unit in a single chip multiprocessor	712/222
37	US 61449 82 A	<input type="checkbox"/>	Pipeline processor and computing system including an apparatus for tracking pipeline resources	718/104
38	US 61449 80 A	<input type="checkbox"/>	Method and apparatus for performing multiple types of multiplication including signed and unsigned multiplication	708/627
39	US 61426 83 A	<input type="checkbox"/>	Debug interface including data steering between a processor, an input/output port, and a trace logic	717/128
40	US 61417 40 A	<input type="checkbox"/>	Apparatus and method for microcode patching for generating a next address	711/215
41	US 61382 31 A	<input type="checkbox"/>	System and method for register renaming	712/216
42	US 61346 51 A	<input type="checkbox"/>	Reorder buffer employed in a microprocessor to store instruction results having a plurality of entries predetermined to correspond to a plurality of functional units	712/215
43	US 61346 45 A	<input type="checkbox"/>	Instruction completion logic distributed among execution units for improving completion efficiency	712/23
44	US 61345 74 A	<input type="checkbox"/>	Method and apparatus for achieving higher frequencies of exactly rounded results	708/551

	Docum ent ID	U	Title	Current OR
45	US 61311 57 A	<input type="checkbox"/>	System and method for retiring approximately simultaneously a group of instructions in a superscalar microprocessor	712/218
46	US 61311 55 A	<input type="checkbox"/>	Programmer-visible uncached load/store unit having burst capability	712/207
47	US 61311 04 A	<input type="checkbox"/>	Floating point addition pipeline configured to perform floating point-to-integer and integer-to-floating point conversion operations	708/204
48	US 61287 23 A	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
49	US 61287 10 A	<input type="checkbox"/>	Method utilizing a set of blocking-symbol resource-manipulation instructions for protecting the integrity of data in noncontiguous data objects of resources in a shared memory of a multiple processor computer system	711/152
50	US 61254 43 A	<input type="checkbox"/>	Interrupt processing system and method for information processing system of pipeline control type	712/244
51	US 61157 33 A	<input type="checkbox"/>	Method and apparatus for calculating reciprocals and reciprocal square roots	708/654
52	US 61157 32 A	<input type="checkbox"/>	Method and apparatus for compressing intermediate products	708/625
53	US 61157 30 A	<input type="checkbox"/>	Reloadable floating point unit	708/505
54	US 61123 17 A	<input type="checkbox"/>	Processor performance counter for sampling the execution frequency of individual instructions	714/47
55	US 61120 19 A	<input type="checkbox"/>	Distributed instruction queue	712/214
56	US 61087 69 A	<input type="checkbox"/>	Dependency table for reducing dependency checking hardware	712/216
57	US 61087 66 A	<input type="checkbox"/>	Structure of processor having a plurality of main processors and sub processors, and a method for sharing the sub processors	712/34
58	US 61065 73 A	<input type="checkbox"/>	Apparatus and method for tracing microprocessor instructions	717/128
59	US 61051 28 A	<input type="checkbox"/>	Method and apparatus for dispatching instructions to execution units in waves	712/215
60	US 61015 97 A	<input type="checkbox"/>	Method and apparatus for maximum throughput scheduling of dependent operations in a pipelined processor	712/218
61	US 61015 94 A	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41
62	US 60981 68 A	<input type="checkbox"/>	System for completing instruction out-of-order which performs target address comparisons prior to dispatch	712/218
63	US 60981 67 A	<input type="checkbox"/>	Apparatus and method for fast unified interrupt recovery and branch recovery in processors supporting out-of-order execution	712/218
64	US 60946 68 A	<input type="checkbox"/>	Floating point arithmetic unit including an efficient close data path	708/505
65	US 60921 81 A	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/206
66	US 60887 90 A	<input type="checkbox"/>	Using a table to track and locate the latest copy of an operand	712/218

	Docum ent ID	U	Title	Current OR
67	US 60887 15 A	<input type="checkbox"/>	Close path selection unit for performing effective subtraction within a floating point arithmetic unit	708/505
68	US 60853 11 A	<input type="checkbox"/>	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/204
69	US 60852 13 A	<input type="checkbox"/>	Method and apparatus for simultaneously multiplying two or more independent pairs of operands and summing the products	708/603
70	US 60852 12 A	<input type="checkbox"/>	Efficient method for performing close path subtraction in a floating point arithmetic unit	708/505
71	US 60852 08 A	<input type="checkbox"/>	Leading one prediction unit for normalizing close path subtraction results within a floating point arithmetic unit	708/205
72	US 60818 87 A	<input type="checkbox"/>	System for passing an index value with each prediction in forward direction to enable truth predictor to associate truth value with particular branch instruction	712/239
73	US 60782 70 A	<input type="checkbox"/>	Data transmission method of a remote controller	340/825 .72
74	US 60761 53 A	<input type="checkbox"/>	Processor pipeline including partial replay	712/23
75	US 60732 17 A	<input type="checkbox"/>	Method for detecting updates to instructions which are within an instruction processing pipeline of a microprocessor	711/146
76	US 60651 12 A	<input type="checkbox"/>	Microprocessor with arithmetic processing units and arithmetic execution unit	712/221
77	US 60651 10 A	<input type="checkbox"/>	Method and apparatus for loading an instruction buffer of a processor capable of out-of-order instruction issue	712/217
78	US 60556 50 A	<input type="checkbox"/>	Processor configured to detect program phase changes and to adapt thereto	714/39
79	US 60527 76 A	<input type="checkbox"/>	Branch operation system where instructions are queued until preparations is ascertained to be completed and branch distance is considered as an execution condition	712/233
80	US 60527 08 A	<input type="checkbox"/>	Performance monitoring of thread switch events in a multithreaded processor	718/108
81	US 60498 63 A	<input type="checkbox"/>	Predecoding technique for indicating locations of opcode bytes in variable byte-length instructions within a superscalar microprocessor	712/213
82	US 60473 70 A	<input type="checkbox"/>	Control of processor pipeline movement through replay queue and pointer backup	712/219
83	US 60444 50 A	<input type="checkbox"/>	Processor for VLIW instruction	712/24
84	US 60442 22 A	<input type="checkbox"/>	System, method, and program product for loop instruction scheduling hardware lookahead	717/156
85	US 60413 98 A	<input type="checkbox"/>	Massively parallel multiple-folded clustered processor mesh array	712/11
86	US 60386 54 A	<input type="checkbox"/>	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
87	US 60386 53 A	<input type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
88	US 60385 83 A	<input type="checkbox"/>	Method and apparatus for simultaneously multiplying two or more independent pairs of operands and calculating a rounded products	708/628
89	US 60353 94 A	<input type="checkbox"/>	System for providing high performance speculative processing of complex load/store instructions by generating primitive instructions in the load/store unit and sequencer in parallel	712/245

	Docum ent ID	U	Title	Current OR
90	US 60353 89 A	<input type="checkbox"/>	Scheduling instructions with different latencies	712/216
91	US 60322 52 A	<input type="checkbox"/>	Apparatus and method for efficient loop control in a superscalar microprocessor	712/233
92	US 60292 44 A	<input type="checkbox"/>	Microprocessor including an efficient implementation of extreme value instructions	712/223
93	US 60264 83 A	<input type="checkbox"/>	Method and apparatus for simultaneously performing arithmetic on two or more pairs of operands	712/221
94	US 60264 82 A	<input type="checkbox"/>	Recorder buffer and a method for allocating a fixed amount of storage for instruction results independent of a number of concurrently dispatched instructions	712/215
95	US 60237 56 A	<input type="checkbox"/>	Instruction processing method and system for variable-length instructions	712/208
96	US 60214 88 A	<input type="checkbox"/>	Data processing system having an apparatus for tracking a status of an out-of-order operation and method thereof	712/228
97	US 60214 85 A	<input type="checkbox"/>	Forwarding store instruction result to load instruction with reduced stall or flushing by effective/real data address bytes matching	712/216
98	US 60214 84 A	<input type="checkbox"/>	Dual instruction set architecture	712/41
99	US 60165 41 A	<input type="checkbox"/>	Instruction controlling system and method thereof	712/217
100	US 60147 41 A	<input type="checkbox"/>	Apparatus and method for predicting an end of a microcode loop	712/233
101	US 60121 41 A	<input type="checkbox"/>	Apparatus for detecting and executing traps in a superscalar processor	712/244
102	US 60095 14 A	<input type="checkbox"/>	Computer method and apparatus for analyzing program instructions executing in a computer system	712/236
103	US 60095 13 A	<input type="checkbox"/>	Apparatus and method for detecting microbranches early	712/231
104	US 60063 24 A	<input type="checkbox"/>	High performance superscalar alignment unit	712/204
105	US 60063 18 A	<input type="checkbox"/>	General purpose, dynamic partitioning, programmable media processor	712/28
106	US 59960 85 A	<input type="checkbox"/>	Concurrent execution of machine context synchronization operations and non-interruptible instructions	713/400
107	US 59960 62 A	<input type="checkbox"/>	Method and apparatus for controlling an instruction pipeline in a data processing system	712/215
108	US 59957 43 A	<input type="checkbox"/>	Method and system for interrupt handling during emulation in a data processing system	703/21
109	US 59875 95 A	<input type="checkbox"/>	Method and apparatus for predicting when load instructions can be executed out-of order	712/216
110	US 59875 93 A	<input type="checkbox"/>	System and method for handling load and/or store operations in a superscalar microprocessor	712/206
111	US 59875 85 A	<input type="checkbox"/>	One-chip microprocessor with error detection on the chip	712/1
112	US 59833 43 A	<input type="checkbox"/>	Data processing system having an apparatus for de-serialized status register operation and method therefor	712/237

	Docum ent ID	U	Title	Current OR
113	US 59833 42 A	<input type="checkbox"/>	Superscalar microprocessor employing a future file for storing results into multiportion registers	712/218
114	US 59833 41 A	<input type="checkbox"/>	Data processing system and method for extending the time for execution of an instruction	712/216
115	US 59833 37 A	<input type="checkbox"/>	Apparatus and method for patching an instruction by providing a substitute instruction or instructions from an external memory responsive to detecting an opcode of the instruction	712/32
116	US 59789 08 A	<input type="checkbox"/>	Computer instruction supply	712/240
117	US 59788 96 A	<input type="checkbox"/>	Method and system for increased instruction dispatch efficiency in a superscalar processor system	712/23
118	US 59745 31 A	<input type="checkbox"/>	Methods and systems of stack renaming for superscalar stack-based data processors	712/202
119	US 59745 22 A	<input type="checkbox"/>	Machine for processing interrupted out-of-order instructions	712/23
120	US 59742 40 A	<input type="checkbox"/>	Method and system for buffering condition code data in a data processing system having out-of-order and speculative instruction execution	712/218
121	US 59681 35 A	<input type="checkbox"/>	Processing instructions up to load instruction after executing sync flag monitor instruction during plural processor shared memory store/load access synchronization	709/400
122	US 59665 44 A	<input type="checkbox"/>	Data speculatable processor having reply architecture	712/32
123	US 59648 68 A	<input type="checkbox"/>	Method and apparatus for implementing a speculative return stack buffer	712/234
124	US 59637 23 A	<input type="checkbox"/>	System for pairing dependent instructions having non-contiguous addresses during dispatch	712/215
125	US 59616 36 A	<input type="checkbox"/>	Checkpoint table for selective instruction flushing in a speculative execution unit	712/228
126	US 59616 34 A	<input type="checkbox"/>	Reorder buffer having a future file for storing speculative instruction execution results	712/218
127	US 59616 29 A	<input type="checkbox"/>	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
128	US 59604 67 A	<input type="checkbox"/>	Apparatus for efficiently providing memory operands for instructions	711/214
129	US 59580 43 A	<input type="checkbox"/>	Superscalar processor with forward map buffer in multiple instruction parallel issue/execution management system	712/216
130	US 59564 95 A	<input type="checkbox"/>	Method and system for processing branch instructions during emulation in a data processing system	703/26
131	US 59548 15 A	<input type="checkbox"/>	Invalidating instructions in fetched instruction blocks upon predicted two-step branch operations with second operation relative target address	712/237
132	US 59535 20 A	<input type="checkbox"/>	Address translation buffer for data processing system emulation mode	703/26
133	US 59516 79 A	<input type="checkbox"/>	Microprocessor circuits, systems, and methods for issuing successive iterations of a short backward branch loop in a single cycle	712/241
134	US 59516 75 A	<input type="checkbox"/>	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/215
135	US 59516 74 A	<input type="checkbox"/>	Object-code compatible representation of very long instruction word programs	712/210

	Docum ent ID	U	Title	Current OR
136	US 59480 60 A	<input type="checkbox"/>	Speeding-up communication rates on links transferring data structures by a method of handing scatter/gather of storage blocks in commanded computer systems	709/212
137	US 59467 05 A	<input type="checkbox"/>	Avoidance of cache synonyms	711/108
138	US 59464 68 A	<input type="checkbox"/>	Reorder buffer having an improved future file for storing speculative instruction execution results	712/218
139	US 59448 11 A	<input type="checkbox"/>	Superscalar processor with parallel issue and execution device having forward map of operand and instruction dependencies	712/23
140	US 59419 84 A	<input type="checkbox"/>	Data processing device	712/218
141	US 59419 83 A	<input type="checkbox"/>	Out-of-order execution using encoded dependencies between instructions in queues to determine stall values that control issuance of instructions from the queues	712/214
142	US 59336 29 A	<input type="checkbox"/>	Apparatus and method for detecting microbranches early	712/248
143	US 59336 27 A	<input type="checkbox"/>	Thread switch on blocked load or store using instruction thread field	712/228
144	US 59336 26 A	<input type="checkbox"/>	Apparatus and method for tracing microprocessor instructions	712/227
145	US 59336 18 A	<input type="checkbox"/>	Speculative register storage for storing speculative results corresponding to register updated by a plurality of concurrently recorded instruction	712/217
146	US 59319 57 A	<input type="checkbox"/>	Support for out-of-order execution of loads and stores in a processor	714/48
147	US 59305 20 A	<input type="checkbox"/>	Pipelining device in a parallel processing apparatus and an instruction supplying method therefor	712/23
148	US 59283 53 A	<input type="checkbox"/>	Clear processing of a translation lookaside buffer with less waiting time	712/200
149	US 59266 45 A	<input type="checkbox"/>	Method and system for enabling multiple store instruction completions in a processing system	712/23
150	US 59251 14 A	<input type="checkbox"/>	Modem implemented in software for operation on a general purpose computer having operating system with different execution priority levels	710/48
151	US 59238 62 A	<input type="checkbox"/>	Processor that decodes a multi-cycle instruction into single-cycle micro-instructions and schedules execution of the micro-instructions	712/208
152	US 59207 10 A	<input type="checkbox"/>	Apparatus and method for modifying status bits in a reorder buffer with a large speculative state	712/216
153	US 59180 62 A	<input type="checkbox"/>	Microprocessor including an efficient implementation of an accumulate instruction	712/7
154	US 59180 46 A	<input type="checkbox"/>	Method and apparatus for a branch instruction pointer table	712/239
155	US 59151 10 A	<input type="checkbox"/>	Branch misprediction recovery in a reorder buffer having a future file	712/239
156	US 59130 59 A	<input type="checkbox"/>	Multi-processor system for inheriting contents of register from parent thread to child thread	718/104
157	US 59130 50 A	<input type="checkbox"/>	Method and apparatus for providing address-size backward compatibility in a processor using segmented memory	711/213
158	US 59130 48 A	<input type="checkbox"/>	Dispatching instructions in a processor supporting out-of-order execution	712/215

	Docum ent ID	U	Title	Current OR
159	US 59130 47 A	<input type="checkbox"/>	Pairing floating point exchange instruction with another floating point instruction to reduce dispatch latency	712/213
160	US 59095 67 A	<input type="checkbox"/>	Apparatus and method for native mode processing in a RISC-based CISC processor	712/208
161	US 59078 60 A	<input type="checkbox"/>	System and method of retiring store data from a write buffer	711/117
162	US 59077 02 A	<input type="checkbox"/>	Method and apparatus for decreasing thread switch latency in a multithread processor	718/108
163	US 59039 18 A	<input type="checkbox"/>	Program counter age bits	711/220
164	US 59037 41 A	<input type="checkbox"/>	Method of allocating a fixed reorder buffer storage line for execution results regardless of a number of concurrently dispatched instructions	712/218
165	US 59037 40 A	<input type="checkbox"/>	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/217
166	US 59013 02 A	<input type="checkbox"/>	Superscalar microprocessor having symmetrical, fixed issue positions each configured to execute a particular subset of instructions	712/215
167	US 59000 24 A	<input type="checkbox"/>	Method for processing type-ahead input and operation-abort input	712/225
168	US 58988 82 A	<input type="checkbox"/>	Method and system for enhanced instruction dispatch in a superscalar processor system utilizing independently accessed intermediate storage	712/23
169	US 58988 65 A	<input type="checkbox"/>	Apparatus and method for predicting an end of loop for string instructions	712/239
170	US 58988 64 A	<input type="checkbox"/>	Method and system for executing a context-altering instruction without performing a context-synchronization operation within high-performance processors	712/228
171	US 58988 52 A	<input type="checkbox"/>	Load instruction steering in a dual data cache microarchitecture	712/214
172	US 58965 18 A	<input type="checkbox"/>	Instruction queue scanning using opcode identification	712/208
173	US 58945 82 A	<input type="checkbox"/>	Method of controlling parallel processing at an instruction level and processor for realizing the method	712/23
174	US 58945 75 A	<input type="checkbox"/>	Method and system for initial state determination for instruction trace reconstruction	717/128
175	US 58929 36 A	<input type="checkbox"/>	Speculative register file for storing speculative register states and removing dependencies between instructions utilizing the register	712/216
176	US 58899 47 A	<input type="checkbox"/>	Apparatus and method for executing instructions that select a storage location for output values in response to an operation count	709/213
177	US 58871 74 A	<input type="checkbox"/>	System, method, and program product for instruction scheduling in the presence of hardware lookahead accomplished by the rescheduling of idle slots	717/161
178	US 58871 61 A	<input type="checkbox"/>	Issuing instructions in a processor supporting out-of-order execution	712/244
179	US 58871 52 A	<input type="checkbox"/>	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
180	US 58840 58 A	<input type="checkbox"/>	Method for concurrently dispatching microcode and directly-decoded instructions in a microprocessor	712/214
181	US 58813 07 A	<input type="checkbox"/>	Deferred store data read with simple anti-dependency pipeline inter-lock control in superscalar processor	712/23

	Docum ent ID	U	Title	Current OR
182	US 58782 44 A	<input type="checkbox"/>	Reorder buffer configured to allocate storage capable of storing results corresponding to a maximum number of concurrently receivable instructions regardless of a number of instructions received	712/218
183	US 58782 42 A	<input type="checkbox"/>	Method and system for forwarding instructions in a processor with increased forwarding probability	712/216
184	US 58731 15 A	<input type="checkbox"/>	Cache memory	711/129
185	US 58729 51 A	<input type="checkbox"/>	Reorder buffer having a future file for storing speculative instruction execution results	712/218
186	US 58729 49 A	<input type="checkbox"/>	Apparatus and method for managing data flow dependencies arising from out-of-order execution, by an execution unit, of an instruction series input from an instruction source	712/216
187	US 58729 46 A	<input type="checkbox"/>	Instruction alignment unit employing dual instruction queues for high frequency instruction dispatch	712/204
188	US 58706 12 A	<input type="checkbox"/>	Method and apparatus for condensed history buffer	710/260
189	US 58705 79 A	<input type="checkbox"/>	Reorder buffer including a circuit for selecting a designated mask corresponding to an instruction that results in an exception	712/217
190	US 58705 77 A	<input type="checkbox"/>	System and method for dispatching two instructions to the same execution unit in a single cycle	712/215
191	US 58705 75 A	<input type="checkbox"/>	Indirect unconditional branches in data processing system emulation mode	712/209
192	US 58685 45 A	<input type="checkbox"/>	Automatic article feeding system	414/808
193	US 58677 34 A	<input type="checkbox"/>	Multiple-reader multiple-writer queue for a computer system	710/52
194	US 58676 98 A	<input type="checkbox"/>	Apparatus and method for accessing a branch target buffer	712/238
195	US 58676 84 A	<input type="checkbox"/>	Method and processor that permit concurrent execution of a store multiple instruction and a dependent instruction	712/218
196	US 58676 82 A	<input type="checkbox"/>	High performance superscalar microprocessor including a circuit for converting CISC instructions to RISC operations	712/210
197	US 58676 80 A	<input type="checkbox"/>	Microprocessor configured to simultaneously dispatch microcode and directly-decoded instructions	712/204
198	US 58646 90 A	<input type="checkbox"/>	Apparatus and method for register specific fill-in of register generic micro instructions within an instruction queue	712/208
199	US 58643 41 A	<input type="checkbox"/>	Instruction dispatch unit and method for dynamically classifying and issuing instructions to execution units with non-uniform forwarding	712/214
200	US 58600 14 A	<input type="checkbox"/>	Method and apparatus for improved recovery of processor state using history buffer	710/260

	Docum ent ID	U	Title	Current OR
1	US 58600 14 A	<input type="checkbox"/>	Method and apparatus for improved recovery of processor state using history buffer	710/260
2	US 58599 98 A	<input type="checkbox"/>	Hierarchical microcode implementation of floating point instructions for a microprocessor	712/222
3	US 58599 92 A	<input type="checkbox"/>	Instruction alignment using a dispatch list and a latch list	712/204
4	US 58570 97 A	<input type="checkbox"/>	Method for identifying reasons for dynamic stall cycles during the execution of a program	712/236
5	US 58570 89 A	<input type="checkbox"/>	Floating point stack and exchange instruction	712/222
6	US 58505 63 A	<input type="checkbox"/>	Processor and method for out-of-order completion of floating-point operations during load/store multiple operations	712/23
7	US 58505 42 A	<input type="checkbox"/>	Microprocessor instruction hedge-fetching in a multiprediction branch environment	712/235
8	US 58451 02 A	<input type="checkbox"/>	Determining microcode entry points and prefix bytes using a parallel logic technique	712/211
9	US 58419 99 A	<input type="checkbox"/>	Information handling system having a register remap structure using a content addressable table	712/217
10	US 58389 40 A	<input type="checkbox"/>	Method and apparatus for rotating active instructions in a parallel data processor	712/216
11	US 58359 68 A	<input type="checkbox"/>	Apparatus for providing memory and register operands concurrently to functional units	711/214
12	US 58322 92 A	<input type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
13	US 58290 21 A	<input type="checkbox"/>	System for controlling operating timing of a cache memory	711/118
14	US 58288 73 A	<input type="checkbox"/>	Assembly queue for a floating point unit	712/222
15	US 58288 68 A	<input type="checkbox"/>	Processor having execution core sections operating at different clock rates	713/501
16	US 58260 96 A	<input type="checkbox"/>	Minimal instruction set computer architecture and multiple instruction issue method	712/24
17	US 58260 73 A	<input type="checkbox"/>	Self-modifying code handling system	712/226
18	US 58260 55 A	<input type="checkbox"/>	System and method for retiring instructions in a superscalar microprocessor	712/218
19	US 58260 53 A	<input type="checkbox"/>	Speculative instruction queue and method therefor particularly suitable for variable byte-length instructions	712/210
20	US 58226 03 A	<input type="checkbox"/>	High bandwidth media processor interface for transmitting data in the form of packets with requests linked to associated responses by identification data	712/1
21	US 58225 74 A	<input type="checkbox"/>	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
22	US 58225 70 A	<input type="checkbox"/>	System and method for parsing and executing a single instruction stream using a plurality of tightly coupled parsing and execution units	703/26
23	US 58225 56 A	<input type="checkbox"/>	Distributed completion control in a microprocessor	712/205

	Docum ent ID	U	Title	Current OR
24	US 58191 14 A	<input type="checkbox"/>	Interruption recovery and resynchronization of events in a computer	710/57
25	US 58130 39 A	<input type="checkbox"/>	Guest execution control system, method and computer process for a virtual machine system	711/156
26	US 58128 11 A	<input type="checkbox"/>	Executing speculative parallel instructions threads with forking and inter-thread communication	712/216
27	US 58093 24 A	<input type="checkbox"/>	Multiple instruction dispatch system for pipelined microprocessor without branch breaks	712/23
28	US 58093 21 A	<input type="checkbox"/>	General purpose, multiple precision parallel operation, programmable media processor	712/1
29	US 58093 20 A	<input type="checkbox"/>	High-performance multi-processor having floating point unit	712/34
30	US 58092 76 A	<input type="checkbox"/>	System and method for register renaming	712/217
31	US 58092 68 A	<input type="checkbox"/>	Method and system for tracking resource allocation within a processor	712/200
32	US 58059 16 A	<input type="checkbox"/>	Method and apparatus for dynamic allocation of registers for intermediate floating-point results	712/23
33	US 58059 06 A	<input type="checkbox"/>	Method and apparatus for writing information to registers in a data processing system using a number of registers for processing instructions	710/260
34	US 58025 56 A	<input type="checkbox"/>	Method and apparatus for correcting misaligned instruction data	711/109
35	US 57969 96 A	<input type="checkbox"/>	Processor apparatus and its control method for controlling a processor having a CPU for executing an instruction according to a control program	712/225
36	US 57940 61 A	<input type="checkbox"/>	General purpose, multiple precision parallel operation, programmable media processor	712/1
37	US 57940 60 A	<input type="checkbox"/>	General purpose, multiple precision parallel operation, programmable media processor	712/1
38	US 57873 03 A	<input type="checkbox"/>	Digital computer system capable of processing a plurality of instructions in parallel based on a VLIW architecture	712/24
39	US 57843 24 A	<input type="checkbox"/>	Single-chip memory system having a multiple bit line structure for outputting a plurality of data simultaneously	365/207
40	US 57782 21 A	<input type="checkbox"/>	System for executing asynchronous branch and link in parallel processor	712/244
41	US 57713 66 A	<input type="checkbox"/>	Method and system for interchanging operands during complex instruction execution in a data processing system	712/217
42	US 57685 76 A	<input type="checkbox"/>	Method and apparatus for predicting and handling resolving return from subroutine instructions in a computer processor	712/238
43	US 57652 21 A	<input type="checkbox"/>	Method and system of addressing which minimize memory utilized to store logical addresses by storing high order bits within a register	711/220
44	US 57652 20 A	<input type="checkbox"/>	Apparatus and method to reduce instruction address storage in a super-scaler processor	711/220
45	US 57652 15 A	<input type="checkbox"/>	Method and system for efficient rename buffer deallocation within a processor	711/214
46	US 57650 16 A	<input type="checkbox"/>	Reorder buffer configured to store both speculative and committed register states	712/23

	Docum ent ID	U	Title	Current OR
47	US 57649 70 A	<input type="checkbox"/>	Method and apparatus for supporting speculative branch and link/branch on count instructions	712/233
48	US 57649 38 A	<input type="checkbox"/>	Resynchronization of a superscalar processor	712/200
49	US 57614 73 A	<input type="checkbox"/>	Method and system for increased instruction synchronization efficiency in a superscalar processor system utilizing partial data dependency interlocking	712/217
50	US 57548 13 A	<input type="checkbox"/>	Data processor	712/216
51	US 57548 11 A	<input type="checkbox"/>	Instruction dispatch queue for improved instruction cache to queue timing	712/214
52	US 57519 95 A	<input type="checkbox"/>	Apparatus and method of maintaining processor ordering in a multiprocessor system which includes one or more processors that execute instructions speculatively	711/145
53	US 57519 81 A	<input type="checkbox"/>	High performance superscalar microprocessor including a speculative instruction queue for byte-aligning CISC instructions stored in a variable byte-length format	712/204
54	US 57489 78 A	<input type="checkbox"/>	Byte queue divided into multiple subqueues for optimizing instruction selection logic	712/23
55	US 57428 40 A	<input type="checkbox"/>	General purpose, multiple precision parallel operation, programmable media processor	712/210
56	US 57427 91 A	<input type="checkbox"/>	Apparatus for detecting updates to instructions which are within an instruction processing pipeline of a microprocessor	711/146
57	US 57427 84 A	<input type="checkbox"/>	System for reordering of instructions before placement into cache to reduce dispatch latency	712/213
58	US 57427 81 A	<input type="checkbox"/>	Decoded instruction buffer apparatus and method for reducing power consumption in a digital signal processor	712/208
59	US 57404 15 A	<input type="checkbox"/>	Instruction supplying apparatus with a branch target buffer having the contents so updated as to enhance branch prediction accuracy	712/238
60	US 57271 77 A	<input type="checkbox"/>	Reorder buffer circuit accommodating special instructions operating on odd-width results	712/218
61	US 57245 65 A	<input type="checkbox"/>	Method and system for processing first and second sets of instructions by first and second types of processing systems	712/245
62	US 57218 57 A	<input type="checkbox"/>	Method and apparatus for saving the effective address of floating point memory operations in an out-of-order microprocessor	712/23
63	US 57062 90 A	<input type="checkbox"/>	Method and apparatus including system architecture for multimedia communication	370/465
64	US 56995 37 A	<input type="checkbox"/>	Processor microarchitecture for efficient dynamic scheduling and execution of chains of dependent instructions	712/217
65	US 56995 36 A	<input type="checkbox"/>	Computer processing system employing dynamic instruction formatting	712/216
66	US 56969 55 A	<input type="checkbox"/>	Floating point stack and exchange instruction	712/222
67	US 56969 39 A	<input type="checkbox"/>	Apparatus and method using a semaphore buffer for semaphore instructions	711/150
68	US 56945 65 A	<input type="checkbox"/>	Method and device for early deallocation of resources during load/store multiple operations to allow simultaneous dispatch/execution of subsequent instructions	712/216
69	US 56921 70 A	<input type="checkbox"/>	Apparatus for detecting and executing traps in a superscalar processor	712/244

	Docum ent ID	U	Title	Current OR
70	US 56897 20 A	<input type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution	712/23
71	US 56825 21 A	<input type="checkbox"/>	Microprocessor control system which selects operating instructions and operands in an order based upon the number of transferred executable operating instructions	712/200
72	US 56805 97 A	<input type="checkbox"/>	System with flexible local control for modifying same instruction partially in different processor of a SIMD computer system to execute dissimilar sequences of instructions	712/226
73	US 56757 76 A	<input type="checkbox"/>	Data processor using FIFO memories for routing operations to parallel operational units	712/220
74	US 56642 15 A	<input type="checkbox"/>	Data processor with an execution unit for performing load instructions and method of operation	712/23
75	US 56641 36 A	<input type="checkbox"/>	High performance superscalar microprocessor including a dual-pathway circuit for converting cisc instructions to risc operations	712/208
76	US 56641 20 A	<input type="checkbox"/>	Method for executing instructions and execution unit instruction reservation table within an in-order completion processor	712/217
77	US 56597 82 A	<input type="checkbox"/>	System and method for handling load and/or store operations in a superscalar microprocessor	712/23
78	US 56550 98 A	<input type="checkbox"/>	High performance superscalar microprocessor including a circuit for byte-aligning cisc instructions stored in a variable byte-length format	712/210
79	US 56550 97 A	<input type="checkbox"/>	High performance superscalar microprocessor including an instruction cache circuit for byte-aligning CISC instructions stored in a variable byte-length format	712/204
80	US 56511 25 A	<input type="checkbox"/>	High performance superscalar microprocessor including a common reorder buffer and common register file for both integer and floating point operations	712/218
81	US 56492 32 A	<input type="checkbox"/>	Structure and method for multiple-level read buffer supporting optimal throttled read operations by regulating transfer rate	710/60
82	US 56492 25 A	<input type="checkbox"/>	Resynchronization of a superscalar processor	712/23
83	US 56491 37 A	<input type="checkbox"/>	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/207
84	US 56363 63 A	<input type="checkbox"/>	Hardware control structure and method for off-chip monitoring entries of an on-chip cache	711/138
85	US 56341 36 A	<input type="checkbox"/>	Data processor and method of controlling the same	712/237
86	US 56338 13 A	<input type="checkbox"/>	Apparatus and method for automatic test generation and fault simulation of electronic circuits, based on programmable logic circuits	703/14
87	US 56300 82 A	<input type="checkbox"/>	Apparatus and method for instruction queue scanning	712/213
88	US 56257 85 A	<input type="checkbox"/>	Information processing apparatus having dual buffers for transmitting debug data to an external debug unit	712/227
89	US 56236 15 A	<input type="checkbox"/>	Circuit and method for reducing prefetch cycles on microprocessors	712/238
90	US 56218 96 A	<input type="checkbox"/>	Data processor with unified store queue permitting hit under miss memory accesses	711/118
91	US 56197 30 A	<input type="checkbox"/>	Pipelining device in a parallel processing apparatus and an instruction supplying method therefor	710/35

	Docum ent ID	U	Title	Current OR
92	US 56196 79 A	<input type="checkbox"/>	Memory control device and method operated in consecutive access mode	711/167
93	US 56196 67 A	<input type="checkbox"/>	Method and apparatus for fast fill of translator instruction queue	712/208
94	US 56130 80 A	<input type="checkbox"/>	Multiple execution unit dispatch with instruction shifting between first and second instruction buffers based upon data dependency	712/214
95	US 56110 63 A	<input type="checkbox"/>	Method for executing speculative load instructions in high-performance processors	712/205
96	US 56066 75 A	<input type="checkbox"/>	Data processor for invalidating prefetched instruction or branch history information	712/237
97	US 56049 09 A	<input type="checkbox"/>	Apparatus for processing instructions in a computing system	712/208
98	US 56048 77 A	<input type="checkbox"/>	Method and apparatus for resolving return from subroutine instructions in a computer processor	712/243
99	US 55948 64 A	<input type="checkbox"/>	Method and apparatus for unobtrusively monitoring processor states and characterizing bottlenecks in a pipelined processor executing grouped instructions	714/39
100	US 55926 79 A	<input type="checkbox"/>	Apparatus and method for distributed control in a processor architecture	712/23
101	US 55926 34 A	<input type="checkbox"/>	Zero-cycle multi-state branch cache prediction data processing system and method thereof	712/239
102	US 55902 95 A	<input type="checkbox"/>	System and method for register renaming	712/217
103	US 55862 95 A	<input type="checkbox"/>	Combination prefetch buffer and instruction cache	711/137
104	US 55840 37 A	<input type="checkbox"/>	Entry allocation in a circular buffer	712/23
105	US 55817 75 A	<input type="checkbox"/>	History buffer system	712/240
106	US 55749 39 A	<input type="checkbox"/>	Multiprocessor coupling system with integrated compile and run time scheduling for parallelism	712/24
107	US 55640 41 A	<input type="checkbox"/>	Microprocessor for inserting a bus cycle in an instruction set to output an internal information for an emulation	703/23
108	US 55617 61 A	<input type="checkbox"/>	Central processing unit data entering and interrogating device and method therefor	714/30
109	US 55600 32 A	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
110	US 55577 63 A	<input type="checkbox"/>	System for handling load and/or store operations in a superscalar microprocessor	712/23
111	US 55532 54 A	<input type="checkbox"/>	Instruction cache access and prefetch process controlled by a predicted instruction-path mechanism	712/207
112	US 55420 58 A	<input type="checkbox"/>	Pipelined computer with operand context queue to simplify context-dependent execution flow	713/502
113	US 55399 11 A	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
114	US 55375 59 A	<input type="checkbox"/>	Exception handling circuit and method	712/244

	Docum ent ID	U	Title	Current OR
115	US 55375 53 A	<input type="checkbox"/>	Method of and apparatus for bus control and data processor	710/100
116	US 55354 10 A	<input type="checkbox"/>	Parallel processor having decoder for selecting switch from the group of switches and concurrently inputting MIMD instructions while performing SIMD operation	712/20
117	US 55308 89 A	<input type="checkbox"/>	Hierarchical structure processor having at least one sub-sequencer for executing basic instructions of a macro instruction	712/247
118	US 55242 55 A	<input type="checkbox"/>	Method and apparatus for accessing global registers in a multiprocessor system	712/203
119	US 55242 21 A	<input type="checkbox"/>	Next instruction pointer calculation system for a microcomputer	712/230
120	US 55176 39 A	<input type="checkbox"/>	System for outputting execution time of industrial automated apparatus	700/108
121	US 55111 75 A	<input type="checkbox"/>	Method an apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/216
122	US 55111 72 A	<input type="checkbox"/>	Speculative execution processor	712/235
123	US 55091 30 A	<input type="checkbox"/>	Method and apparatus for grouping multiple instructions, issuing grouped instructions simultaneously, and executing grouped instructions in a pipelined processor	712/215
124	US 55035 16 A	<input type="checkbox"/>	Automatic article feeding system	414/800
125	US 55009 43 A	<input type="checkbox"/>	Data processor with rename buffer and FIFO buffer for in-order instruction completion	712/218
126	US 54918 29 A	<input type="checkbox"/>	Method and system for indexing the assignment of intermediate storage buffers in a superscalar processor system	712/23
127	US 54887 30 A	<input type="checkbox"/>	Register conflict scoreboard in pipelined computer using pipelined reference counts	712/41
128	US 54817 43 A	<input type="checkbox"/>	Minimal instruction set computer architecture and multiple instruction issue method	712/23
129	US 54816 89 A	<input type="checkbox"/>	Conversion of internal processor register commands to I/O space addresses	711/202
130	US 54715 91 A	<input type="checkbox"/>	Combined write-operand queue and read-after-write dependency scoreboard	712/217
131	US 54653 73 A	<input type="checkbox"/>	Method and system for single cycle dispatch of multiple instructions in a superscalar processor system	712/215
132	US 54653 72 A	<input type="checkbox"/>	Dataflow computer for following data dependent path processes	712/25
133	US 54524 27 A	<input type="checkbox"/>	Data processing device for variable word length instruction system having short instruction execution time and small occupancy area	712/210
134	US 54505 55 A	<input type="checkbox"/>	Register logging in pipelined computer using register log queue of register content changes and base queue of register log queue pointers for respective instructions	712/228
135	US 54386 70 A	<input type="checkbox"/>	Method of prechecking the validity of a write access request	711/3
136	US 54370 17 A	<input type="checkbox"/>	Method and system for maintaining translation lookaside buffer coherency in a multiprocessor data processing system	709/213
137	US 54349 85 A	<input type="checkbox"/>	Simultaneous prediction of multiple branches for superscalar processing	712/240

	Docum ent ID	U	Title	Current OR
138	US 54189 73 A	<input type="checkbox"/>	Digital computer system with cache controller coordinating both vector and scalar operations	712/3
139	US 54148 22 A	<input type="checkbox"/>	Method and apparatus for branch prediction using branch prediction table with improved branch prediction effectiveness	712/240
140	US 54044 71 A	<input type="checkbox"/>	Method and apparatus for switching address generation modes in CPU having plural address generation modes	712/207
141	US 53945 29 A	<input type="checkbox"/>	Branch prediction unit for high-performance processor	712/240
142	US 53923 91 A	<input type="checkbox"/>	High performance graphics applications controller	345/503
143	US 53815 32 A	<input type="checkbox"/>	Microprocessor having branch aligner between branch buffer and instruction decoder unit for enhancing initiation of data processing after execution of conditional branch instruction	712/237
144	US 53815 31 A	<input type="checkbox"/>	Data processor for selective simultaneous execution of a delay slot instruction and a second subsequent instruction the pair following a conditional branch instruction	712/235
145	US 53801 38 A	<input type="checkbox"/>	Automatic article feeding system	414/277
146	US 53496 56 A	<input type="checkbox"/>	Task scheduling method in a multiprocessor system where task selection is determined by processor identification and evaluation information	718/102
147	US 53353 30 A	<input type="checkbox"/>	Information processing apparatus with optimization programming	712/241
148	US 53332 96 A	<input type="checkbox"/>	Combined queue for invalidates and return data in multiprocessor system	711/171
149	US 53177 20 A	<input type="checkbox"/>	Processor system with writeback cache using writeback and non writeback transactions stored in separate queues	711/143
150	US 53177 11 A	<input type="checkbox"/>	Structure and method for monitoring an internal cache	714/47
151	US 53136 02 A	<input type="checkbox"/>	Multiprocessor system and method of control over order of transfer of data between buffer storages	711/100
152	US 53054 58 A	<input type="checkbox"/>	Multiple virtual storage system and address control apparatus having a designation table holding device and translation buffer	711/207
153	US 52993 18 A	<input type="checkbox"/>	Processor with a plurality of microprogrammed units, with anticipated execution indicators and means for executing instructions in pipeline manner	712/231
154	US 52936 02 A	<input type="checkbox"/>	Multiprocessor computer system with dedicated synchronizing cache	711/147
155	US 52874 66 A	<input type="checkbox"/>	Method and apparatus for parallel loads equalizing utilizing instruction sorting by columns based on predicted instruction execution time	712/206
156	US 52673 50 A	<input type="checkbox"/>	Method for fetching plural instructions using single fetch request in accordance with empty state of instruction buffers and setting of flag latches	712/205
157	US 52652 13 A	<input type="checkbox"/>	Pipeline system for executing predicted branch target instruction in a cycle concurrently with the execution of branch instruction	712/240
158	US 52513 06 A	<input type="checkbox"/>	Apparatus for controlling execution of a program in a computing device	712/217
159	US 52416 44 A	<input type="checkbox"/>	Queue having long word length	710/54
160	US 52336 96 A	<input type="checkbox"/>	Microprocessor having precoder unit and main decoder unit operating in pipeline processing manner	712/204

	Docum ent ID	U	Title	Current OR
161	US 52323 31 A	<input type="checkbox"/>	Automatic article feeding system	414/802
162	US 52261 32 A	<input type="checkbox"/>	Multiple virtual addressing using/comparing translation pairs of addresses comprising a space address and an origin address (ST0) while using space registers as storage devices for a data processing system	711/209
163	US 52186 78 A	<input type="checkbox"/>	System and method for atomic access to an input/output device with direct memory access	710/5
164	US 52029 67 A	<input type="checkbox"/>	Data processing apparatus for performing parallel decoding and parallel execution of a variable word length instruction	712/212
165	US 52010 57 A	<input type="checkbox"/>	System for extracting low level concurrency from serial instruction streams	712/18
166	US 51971 45 A	<input type="checkbox"/>	Buffer storage system using parallel buffer storage units and move-out buffer registers	711/143
167	US 51971 31 A	<input type="checkbox"/>	Instruction buffer system for switching execution of current instruction to a branch or to a return from subroutine	712/238
168	US 51858 71 A	<input type="checkbox"/>	Coordination of out-of-sequence fetching between multiple processors using re-execution of instructions	712/205
169	US 51858 68 A	<input type="checkbox"/>	Apparatus having hierarchically arranged decoders concurrently decoding instructions and shifting instructions not ready for execution to vacant decoders higher in the hierarchy	712/217
170	US 51795 30 A	<input type="checkbox"/>	Architecture for integrated concurrent vector signal processor	708/520
171	US 51631 39 A	<input type="checkbox"/>	Instruction preprocessor for conditionally combining short memory instructions into virtual long instructions	712/206
172	US 51573 88 A	<input type="checkbox"/>	Method and apparatus for graphics data interpolation	345/673
173	US 51558 43 A	<input type="checkbox"/>	Error transition mode for multi-processor system	714/5
174	US 51426 31 A	<input type="checkbox"/>	System for queuing individual read or write mask and generating respective composite mask for controlling access to general purpose register	712/217
175	US 51310 86 A	<input type="checkbox"/>	Method and system for executing pipelined three operand construct	712/213
176	US 51250 79 A	<input type="checkbox"/>	Method for controlling the data transmission of a central unit interfacing control circuit and circuit arrangement for the implementation of the method	710/305
177	US 51154 96 A	<input type="checkbox"/>	Queue device capable of quickly transferring a digital signal unit of a word length different from a single word length	711/212
178	US 51013 46 A	<input type="checkbox"/>	Virtual machine system having a plurality of real instruction processors and virtual machines, and a registration table	718/100
179	US 51013 41 A	<input type="checkbox"/>	Pipelined system for reducing instruction access time by accumulating predecoded instruction bits a FIFO	712/213
180	US 50816 98 A	<input type="checkbox"/>	Method and apparatus for graphics display data manipulation	345/422
181	US 50500 76 A	<input type="checkbox"/>	Prefetching queue control system	712/219
182	US RE336 29 E	<input type="checkbox"/>	Numeric data processor	708/510

	Docum ent ID	U	Title	Current OR
183	US 50290 80 A	<input type="checkbox"/>	Method and apparatus for composing a set of instructions for executing a data flow program defined by structured data	712/201
184	US 50181 45 A	<input type="checkbox"/>	IC tester	714/743
185	US 49929 38 A	<input type="checkbox"/>	Instruction control mechanism for a computing system with register renaming, map table and queues indicating available registers	712/217
186	US 49741 98 A	<input type="checkbox"/>	Vector processing system utilizing firm ware control to prevent delays during processing operations	712/8
187	US 49741 54 A	<input type="checkbox"/>	Computer with instruction prefetch queue retreat unit	712/240
188	US 49532 25 A	<input type="checkbox"/>	Handwritten character-recognizing apparatus for automatically generating and displaying character frames	382/179
189	US 49531 21 A	<input type="checkbox"/>	Circuitry for and method of controlling an instruction buffer in a data-processing system	712/241
190	US 49106 57 A	<input type="checkbox"/>	Microprocessor providing bus access for unconditional instruction execution	712/207
191	US 48932 33 A	<input type="checkbox"/>	Method and apparatus for dynamically controlling each stage of a multi-stage pipelined data unit	712/244
192	US 48581 05 A	<input type="checkbox"/>	Pipelined data processor capable of decoding and executing plural instructions in parallel	712/235
193	US 48581 04 A	<input type="checkbox"/>	Preceding instruction address based branch prediction in a pipelined processor	712/240
194	US 48477 53 A	<input type="checkbox"/>	Pipelined computer	712/238
195	US 48477 48 A	<input type="checkbox"/>	Virtual memory arrangement data processing system with decoding and execution of prefetched instructions in parallel	712/212
196	US 48315 15 A	<input type="checkbox"/>	Information processing apparatus for determining sequence of parallel executing instructions in response to storage requirements thereof	712/217
197	US 47665 66 A	<input type="checkbox"/>	Performance enhancement scheme for a RISC type VLSI processor using dual execution units for parallel instruction processing	712/23
198	US 47617 31 A	<input type="checkbox"/>	Look-ahead instruction fetch control for a cache memory	711/156
199	US 47589 49 A	<input type="checkbox"/>	Information processing apparatus	712/208
200	US 47424 53 A	<input type="checkbox"/>	Pipeline-controlled information processing system for generating updated condition code	712/234